Chapter 10

Circuits

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10.1 Introduction

10.1.1 Length, mass, and time in the SI system

From basic mechanics, the reader should already be familiar with the fundamental units of {length, mass, time} as {meter (m), kilogram (kg), second (s)} in the International System of Units (SI, the modern form of the metric system), as well as several derived units, such as force (newton, N = kg m/s^2), pressure (pascal, Pa = kg/m/s^2), energy or work (joule, J = N m), power (watt, W = J/s), frequency (hertz, Hz = 1/s), speed (m/s), acceleration (m/s^2), angular velocity (rad/s) and acceleration (rad/s^2), momentum (N s), angular momentum (N m s), torque (N m), etc. Recall also the usual prefixes of the SI system (cf. the binary powers in Table 1.1):

prefix:	deci	centi	milli	micro	nano	pico	femto	atto	zepto	yocto
symbol:	d	c	m	μ	n	p	f	a	z	y
factor:	10^{-1}	10^{-2}	10^{-3}	10^{-6}	10^{-9}	10^{-12}	10^{-15}	10^{-18}	10^{-21}	10^{-24}

prefix:	deca	hecto	kilo	mega	giga	tera	peta	exa	zetta	yotta
symbol:	da	h	k	M	G	T	P	E	Z	Y
factor:	10^{1}	10^{2}	10^{3}	10^{6}	10^{9}	10^{12}	10^{15}	10^{18}	10^{21}	10^{24}

10.1.2 Electric charge, energy, power, and potential in the SI system

The SI units of the various quantities encountered in electric circuits is now summarized:

- **Charge** is denoted q. The fundamental unit of charge is that of an electron; the (negative) charge of 6.2415×10^{18} electrons is called a **coulomb** (C), which is the SI unit for charge.
- Electric charge passing a given point per unit time is called **current**. The current at any instant is denoted $I = dq/dt$. The SI unit for current is the **ampere** (A, a.k.a. **amp**), which is a flow of 1 C/s.
- **Energy** (aka **work**) is denoted w, and the SI unit for (mechanical or electrical) energy is the **joule** (J). In mechanical terms, a joule of energy is 1 kg m^2/s^2, which may be interpreted as 1 N m when applying a force to a mass over a distance, or as 0.2390 calories of thermal energy, where 1 **calorie** (cal) is the amount of thermal energy it takes to warm 1 g (that is, 1 mL, or 1 cm^3) of water by 1°C at standard atmospheric conditions. Electric energy, also measured in joules, is the electric equivalent, as electrical energy can easily be converted to heat, or to mechanical energy (to apply a force over a distance) plus heat.
- **Power** is the rate of change of energy at any instant (that is, energy is the integral of power over time), and is denoted $P = dw/dt$; the SI unit for power is the **watt** (W), which is 1 J / s. In mechanical terms, a watt of power is 1 kg m^2 / s^3, which may be interpreted as 1 N m / s when applying a force to a mass moving at a certain speed, or as 0.2390 cal / s when warming a material.
- In an electric circuit, associated with any electron is its potential to do work[1] relative to some convenient (yet, arbitrarily-defined) base state, called the **ground** state. This definition is analogous to the gravitational potential energy associated with any mass at any given height relative to an (arbitrarily-defined) gravitational ground state. The **potential** of a charge to do work, also called the **voltage** of this charge, is denoted $V = dw/dq$, and is defined analogously, relative to an (arbitrarily-defined) electrical ground state. The SI unit for potential is the **volt** (V), which is 1 J / C.

Via the above definitions and the chain rule for differentiation, it follows immediately that

$$P = \frac{dw}{dt} = \frac{dw}{dq}\frac{dq}{dt} \quad \Rightarrow \quad \boxed{P = VI} \tag{10.1}$$

Current may be envisioned as a flow of electrons, as described above; however, by convention, the (positive) direction of the current is defined as the direction *opposite* to the flow of electrons. This is known as the **passive sign convention**. Using this (at first, somewhat peculiar[2]) convention, when considering the voltage V across a device and the current I through a device, multiplying V times I as suggested by (10.1) results in

- *positive* power P if the device *absorbs* electric power from the rest of the circuit, as in a resistor[3], with current flowing from *higher* voltage to *lower* voltage, and
- *negative* power P if the device *delivers* electric power to the rest of the circuit, as in a battery, with current flowing from *lower* voltage to *higher* voltage.

As a departure from the SI convention, on the electric grid of a city, energy is usually billed in **kilowatt hours** (kW h) instead of megajoules (MJ); note that 1 kW h = 3.6 MJ. Similarly, battery charge is usually measured as **milliamp hours** (mA h) instead of coulombs (C); note that 1 mA h = 3.6 C.

[1] As an example, consider two identical metal spheres, one with an excess of electrons (said to be of lower voltage), and one with a depletion of electrons (said to be of higher voltage). If a resistor is connected between the two spheres, the excess repulsive force between the electrons on the first sphere tends to push electrons through the resistor and onto the second sphere until a balanced distribution of electrons is reached. In the process, the electrons being pushed through the resistor do work, generating heat.

[2] The reason for this peculiar convention is that the fundamental charge associated with an electron is defined as being *negative*; this definition was made early on, and it stuck.

[3] The power absorbed may be converted into **heat**, as in a resistor, a combination of **heat & electromagnetic radiation**, as in a lightbulb, laser, or RF transmitter, a combination of **heat & mechanical power**, as in a motor, fluid pump, or speaker coil, etc., or it may alternatively be *stored* (and, later, released), as in a capacitor or inductor (see §10.1.3.1), a rechargeable battery, a flywheel, etc.

The change of energy of a single electron if it is moved across a potential difference of one volt is defined as an **electron volt** (eV), and is given by $1/(6.2415 \times 10^{18}) = 1.6022 \times 10^{-19}$ J. Note that the energy E of a **photon** is given by $E = hc/\lambda$, where **Planck's constant** $h = 6.626 \times 10^{-34}$ J s and the **speed of light** $c = 2.99792 \times 10^{8}$ m / s; thus, if a single electron moves across a 1.91 V potential difference, then releases its excess energy as a photon, the resulting photon has wavelength $\lambda = 650$ nm, and is thus red in color.

10.1.3 Fundamental analog circuit elements

10.1.3.1 Resistors, capacitors, & inductors

Idealized current-voltage relationships for three common devices[4] used in analog circuits are

resistor (denoted —/\/\/\—): $\boxed{V = R\,I} \quad \Rightarrow \quad P_{\mathsf{R}} = VI = I^2\,R = V^2/R \geq 0,$ (10.2a)

capacitor (denoted —┤├—): $\boxed{I = C\,dV/dt} \quad \Rightarrow \quad P_{\mathsf{C}} = VI = (C/2)\,dV^2/dt = dw_C/dt,$ (10.2b)

inductor (denoted ⌒⌒⌒): $\boxed{V = L\;dI/dt} \quad \Rightarrow \quad P_{\mathsf{L}} = VI = (L/2)\,dI^2/dt = dw_L/dt,$ (10.2c)

where $w_C = C\,V^2/2$ and $w_L = L\,I^2/2$. Approximate values of R, C, and L for such devices are identified with **color bands** or **numerical codes**, the interpretation of which are easy to find online. Note that:

- The SI unit for resistance R is the **ohm** (Ω) [thus, (10.2a) is known as **Ohm's law**]; an ohm is 1 V / A.
- The SI unit for capacitance C is the **farad** (F); a farad is 1 A s / V.
- The SI unit for inductance L is the **henry** (H); a henry is 1 V s / A.

When operating, electric power is always *absorbed* (i.e., dissipated as heat) by a resistor, but at any instant may either be *absorbed from* or *delivered to* the rest of the circuit by a capacitor or inductor [see (10.2)].

The idealized linear models listed above are accurate only for sufficiently small V and I inside what are known as the **rated limits** of the corresponding device; outside these limits, nonlinearities become significant (and, far outside these limits, the corresponding device will fail).

The flow of electrons along a metal wire, like that of water through a pipe, is almost always[5] associated with some loss of potential per unit length (and, therefore, some resistance), as energy is lost as heat to sustain the flow when the magnetic fields generated by the flowing electrons interact with the electromagnetic fields of the atoms within the material. *Wires* are simply made from an appropriate metal, like copper, with relatively *low* (often, negligible) resistance per unit length, whereas *resistors* are made from an appropriate metal, like Nichrome (a non-magnetic alloy of nickel and chromium), that exhibits a relatively *high* resistance per unit length, with a resistance that is fairly insensitive to the inevitable temperature fluctuations caused by driving a current through a resistor. Note that, when running a large current through a resistor, the metal warms up, and thus atoms within the metal start vibrating more energetically; this generally reduces the effective resistance R of the resistor when $|I|$ is large, eventually leading to a nonlinear relationship between V and I [cf. (10.2a)].

Though they are packaged in a variety of compact geometries, *capacitors* are perhaps best visualized as two parallel metal plates with a nonconducting material, called a **dielectric**, between them. If a current is directed through a capacitor, electrons flow in one wire and accumulate on one of the plates, repelling the electrons on the other (nearby) plate, which then flow out the other wire. As electrons accumulate on the first plate and are depleted from the second, an *electric potential difference* is gradually built up, thus inhibiting the further flow of electrons; at steady state, the current through the capacitor therefore reduces to zero.

[4] As suggested by Thomas & Rosa (2010), we will refer to the physical hardware components that a circuit is made from as **devices**, and the equations we use to model them as **elements**.

[5] The exception to this statement is the remarkable class of materials known as **superconductors**, which at temperatures below a material-dependent critical temperature exhibit **zero resistance** and the expulsion of magnetic fields from within the material.

The resulting (linearized) relationship between between V and I is given in (10.2b). As shown in (10.2b), the power absorbed by or released from a capacitor at any instant, P_C, is simply the rate of change of the energy, $w_C = C\,V^2/2$, stored[6] in the capacitor, where V is the voltage across the capacitor, which quantifies the accumulated charge difference across its two plates. Further, if the current through the capacitor is $I = \cos(\omega t) = \sin(\omega t + \pi/2)$, then the voltage across the capacitor is $V = (1/C)\sin(\omega t)/\omega$ [the voltage "lags" behind the current by $\pi/2$, and its magnitude reduces like $1/\omega$, as the charge difference between the two sides of the capacitor takes time to accumulate; think of the current variation as the "cause", and the voltage variation as the "effect"]. The absorbed power P_C, averaged over any multiple of periods $T = 2\pi/\omega$, is exactly zero.

Conversely, *inductors* are perhaps best visualized as tightly-wound (often, toroidal) copper wire coils wrapped around an air or (better) a ferromagnetic **core**; when a current flows through the wire, a compatible magnetic field is maintained within this core. If a voltage is applied across an inductor, the existing magnetic field in the core, or lack thereof, exerts an *electromotive force* on the flow of electrons which initially opposes a corresponding change in the current. As a voltage difference is maintained across the inductor (which, in turn, is generated by the circuit that is connected to it), the current through the inductor, and the corresponding magnetic field, grows in response; at steady state, the voltage across the inductor reduces to zero[7]. The resulting (linearized) relationship between between V and I is given in (10.2c). As shown in (10.2c), the power absorbed by or released from an inductor at any instant, P_L, is simply the rate of change of the energy, $w_L = L\,I^2/2$, stored[7] in the inductor, where I is the current through the inductor, which quantifies the accumulated magnetic field through its core. Further, if the voltage across an inductor is $V = \cos(\omega t) = \sin(\omega t + \pi/2)$, then the current through the inductor is $I = (1/L)\sin(\omega t)/\omega$ [the current "lags" behind the voltage by $\pi/2$, and its magnitude reduces like $1/\omega$, as the magnetic field within its core takes time to accumulate, and the corresponding electromotive force opposes a change in the current; think of the voltage variation as the "cause", and the current variation as the "effect"]. The absorbed power P_L, averaged over any multiple of periods $T = 2\pi/\omega$, is exactly zero.

The prepackaged resistors, capacitors, and inductors that are commercially available are manufactured with significant variation. Resistors are commonly available with the following tolerances on their nominal resistance: $\{\pm 20\%,\ \pm 10\%,\ \pm 5\%,\ \pm 2\%,\ \pm 1\%,\ \pm 0.5\%,\ \pm 0.25\%,\ \pm 0.1\%\}$. Associated with each of these tolerance levels is a family of resistance values denoted Ex, where x is the number of resistance values per decade that are available in that family, as listed in Tables 10.1-10.6. Available resistors in, e.g., the E6 family include 1.0 kΩ, 1.5 kΩ, 2.2 kΩ, 3.3 kΩ, 4.7 kΩ, 6.8 kΩ, 10 kΩ, 15 kΩ etc. The process of converting (rounding up or down) a given resistance to a value in one of these families is, of course, easily automated (see RR_common_resistor_values.m). Note that higher-precision resistors are more expensive and less commonly stocked at PCB fabrication facilities, and should be avoided. Note also that **calibration** may be used to eliminate the error associated with the use of lower-precision (less expensive) resistors in, e.g., voltage divider circuits, as discussed in §5.7.4.

Resistors at various tolerance levels are often produced as the result of a single manufacturing process, then tested to determine their precise resistance (using, for example, the Wheatstone bridge circuit analyzed in Example 10.5). They are then binned accordingly and, of course, those resistors most closely matching the target resistance of the higher-precision class sold at a higher price. The result of this manufacturing/sorting process is that the distribution of the actual resistance of those resistors marked at, say, 2% tolerance are often **bimodal**, as those units that more accurately match target resistance values at 1% tolerance are not placed in the higher-tolerance (2%) bins. The manufacture of (more expensive) high-precision resistors is often accomplished by accurate **laser trimming** of resistors that are initially slightly below the target resistance.

[6] A mechanical spring stores and releases the energy associated with its compression; as a rough analog, a capacitor can be thought of as a sort of "spring" on the voltage, storing and releasing the energy associated with an accumulated charge, whereas an inductor can be thought of as a "spring" on the current, storing and releasing the energy associated with an accumulated magnetic field.

[7] As a mnemonic, a *capacitor has low voltage across it at high frequencies*, as electric charge doesn't have enough time build up on it, whereas an *inductor has low current through it at high frequencies*, as a compatible magnetic field doesn't have time to form.

1.0	**1.5**	**2.2**	**3.3**	**4.7**	**6.8**

Table 10.1: The 6 resistance values per decade in the **E6** family of $\pm 20\%$ tolerance resistors.

1.0	**1.2**	**1.5**	**1.8**	**2.2**	**2.7**	**3.3**	**3.9**	**4.7**	**5.6**	**6.8**	**8.2**

Table 10.2: The 12 resistance values per decade in the **E12** family of $\pm 10\%$ tolerance resistors.

1.0	**1.1**	**1.2**	**1.3**	**1.5**	**1.6**	**1.8**	**2.0**	**2.2**	**2.4**	**2.7**	**3.0**
3.3	**3.6**	**3.9**	**4.3**	**4.7**	**5.1**	**5.6**	**6.2**	**6.8**	**7.5**	**8.2**	**9.1**

Table 10.3: The 24 resistance values per decade in the **E24** family of $\pm 5\%$ tolerance resistors.

1.00	**1.05**	**1.10**	**1.15**	**1.21**	**1.27**	**1.33**	**1.40**	**1.47**	**1.54**	**1.62**	**1.69**	**1.78**	**1.87**	**1.96**	**2.05**
2.15	**2.26**	**2.37**	**2.49**	**2.61**	**2.74**	**2.87**	**3.01**	**3.16**	**3.32**	**3.48**	**3.65**	**3.83**	**4.02**	**4.22**	**4.42**
4.64	**4.87**	**5.11**	**5.36**	**5.62**	**5.90**	**6.19**	**6.49**	**6.81**	**7.15**	**7.50**	**7.87**	**8.25**	**8.66**	**9.09**	**9.53**

Table 10.4: The 48 resistance values per decade in the **E48** family of $\pm 2\%$ tolerance resistors.

1.00	**1.02**	**1.05**	**1.07**	**1.10**	**1.13**	**1.15**	**1.18**	**1.21**	**1.24**	**1.27**	**1.30**	**1.33**	**1.37**	**1.40**	**1.43**
1.47	**1.50**	**1.54**	**1.58**	**1.62**	**1.65**	**1.69**	**1.74**	**1.78**	**1.82**	**1.87**	**1.91**	**1.96**	**2.00**	**2.05**	**2.10**
2.15	**2.21**	**2.26**	**2.32**	**2.37**	**2.43**	**2.49**	**2.55**	**2.61**	**2.67**	**2.74**	**2.80**	**2.87**	**2.94**	**3.01**	**3.09**
3.16	**3.24**	**3.32**	**3.40**	**3.48**	**3.57**	**3.65**	**3.74**	**3.83**	**3.92**	**4.02**	**4.12**	**4.22**	**4.32**	**4.42**	**4.53**
4.64	**4.75**	**4.87**	**4.99**	**5.11**	**5.23**	**5.36**	**5.49**	**5.62**	**5.76**	**5.90**	**6.04**	**6.19**	**6.34**	**6.49**	**6.65**
6.81	**6.98**	**7.15**	**7.32**	**7.50**	**7.68**	**7.87**	**8.06**	**8.25**	**8.45**	**8.66**	**8.87**	**9.09**	**9.31**	**9.53**	**9.76**

Table 10.5: The 96 resistance values per decade in the **E96** family of $\pm 1\%$ tolerance resistors.

1.00	**1.01**	**1.02**	**1.04**	**1.05**	**1.06**	**1.07**	**1.09**	**1.10**	**1.11**	**1.13**	**1.14**	**1.15**	**1.17**	**1.18**	**1.20**
1.21	**1.23**	**1.24**	**1.26**	**1.27**	**1.29**	**1.30**	**1.32**	**1.33**	**1.35**	**1.37**	**1.38**	**1.40**	**1.42**	**1.43**	**1.45**
1.47	**1.49**	**1.50**	**1.52**	**1.54**	**1.56**	**1.58**	**1.60**	**1.62**	**1.64**	**1.65**	**1.67**	**1.69**	**1.72**	**1.74**	**1.76**
1.78	**1.80**	**1.82**	**1.84**	**1.87**	**1.89**	**1.91**	**1.93**	**1.96**	**1.98**	**2.00**	**2.03**	**2.05**	**2.08**	**2.10**	**2.13**
2.15	**2.18**	**2.21**	**2.23**	**2.26**	**2.29**	**2.32**	**2.34**	**2.37**	**2.40**	**2.43**	**2.46**	**2.49**	**2.52**	**2.55**	**2.58**
2.61	**2.64**	**2.67**	**2.71**	**2.74**	**2.77**	**2.80**	**2.84**	**2.87**	**2.91**	**2.94**	**2.98**	**3.01**	**3.05**	**3.09**	**3.12**
3.16	**3.20**	**3.24**	**3.28**	**3.32**	**3.36**	**3.40**	**3.44**	**3.48**	**3.52**	**3.57**	**3.61**	**3.65**	**3.70**	**3.74**	**3.79**
3.83	**3.88**	**3.92**	**3.97**	**4.02**	**4.07**	**4.12**	**4.17**	**4.22**	**4.27**	**4.32**	**4.37**	**4.42**	**4.48**	**4.53**	**4.59**
4.64	**4.70**	**4.75**	**4.81**	**4.87**	**4.93**	**4.99**	**5.05**	**5.11**	**5.17**	**5.23**	**5.30**	**5.36**	**5.42**	**5.49**	**5.56**
5.62	**5.69**	**5.76**	**5.83**	**5.90**	**5.97**	**6.04**	**6.12**	**6.19**	**6.26**	**6.34**	**6.42**	**6.49**	**6.57**	**6.65**	**6.73**
6.81	**6.90**	**6.98**	**7.06**	**7.15**	**7.23**	**7.32**	**7.41**	**7.50**	**7.59**	**7.68**	**7.77**	**7.87**	**7.96**	**8.06**	**8.16**
8.25	**8.35**	**8.45**	**8.56**	**8.66**	**8.76**	**8.87**	**8.98**	**9.09**	**9.20**	**9.31**	**9.42**	**9.53**	**9.65**	**9.76**	**9.88**

Table 10.6: The resistance values in the **E192** families of $\pm 0.5\%$, $\pm 0.25\%$, and $\pm 0.1\%$ tolerance resistors.

Capacitors are commonly available[8] from 1 pF through 10 nF in 24 capacitance values per decade (coinciding in values with the E24 series in Table 10.3), and from 10 nF=0.01 μF through 10 mF=10^4 μF in 6 capacitance values per decade (coinciding in values with the E6 series in Table 10.1). Inductors are commonly available[8] from 1 nH through 1 mH in 24 inductance values per decade (coinciding in values with the E24 series in Table 10.3). Capacitors and inductors in the higher ends of these ranges are both large and expensive; increased voltage ratings on capacitors, and increased current ratings on inductors, also increase their size and cost significantly.

10.1.3.2 Power sources

In order to make an electric circuit do something, of course, you need a source[9] of electric power. Such sources come in two types, voltage sources (which are most common) and current sources, either of which may drive the connected circuit in a constant or time-varying manner, and are denoted as indicated in Figure 10.1a-d.

[8] Time constants in RLC circuits (incorporating resistors, inductors, and capacitors) may be tuned by selecting the resistors in the circuit (see, e.g., Example 10.2), so a finer granularity in available values per decade is not necessary for capacitors and inductors.

[9] Note that some devices that normally act as *sources* of electric power, like rechargeable batteries, may also from time to time be used safely as *sinks* of electric power, like a capacitor. The practical distinction between a capacitor and a rechargeable battery is that a capacitor, which simply stores and releases electrons, typically loses its charge fairly quickly when not being used, whereas a battery, which stores and releases charge via internal chemical reactions, typically holds its charge for much longer periods of time.

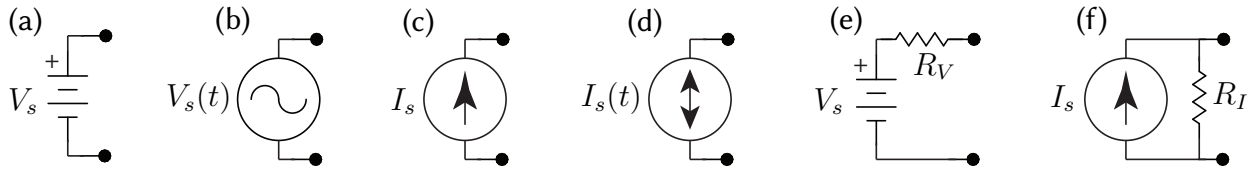


Figure 10.1: Various power sources, and the symbols used for them in this text: (a) ideal constant-voltage source, (b) ideal time-varying voltage source, (c) ideal constant-current source, (d) ideal time-varying current source, (e) practical constant-voltage source, (f) practical constant-current source.

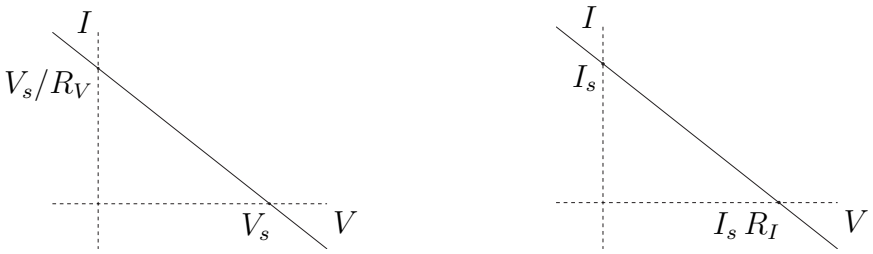


Figure 10.2: Current-voltage relationship of (left) the practical voltage source of Figure 10.1e, and (right) the practical current source of Figure 10.1f.

The current-voltage relationships of ideal voltage and current sources may be written

ideal voltage source: $\boxed{V = V_s \text{ (regardless of } I)}$ **ideal current source**: $\boxed{I = I_s \text{ (regardless of } V)}$ (10.2d)

Note that an ideal **voltage source** generates a specified *voltage* across its terminals[10] regardless of the current drawn by the rest of the circuit; an ideal voltage source can not function correctly if a wire (with zero resistance) is connected across its terminals (a.k.a. a **short circuit**), as that would cause the ideal voltage source to produce infinite current. Similarly, an ideal **current source** generates a specified *current* through the device(s) connected across its terminals regardless of the voltage required over the rest of the circuit in order to maintain it; an ideal current source can not function correctly if the circuit connected across its terminals is not closed (a.k.a. an **open circuit**), as that would cause the ideal current source to produce infinite voltage.

Despite the above-mentioned limitations, ideal voltage and current sources are reasonably good models in many situations when a circuit is properly configured. More accurate (yet still linear) models of real-world voltage and current sources are indicated in Figure 10.1e-f. In these more practical models,

- a (preferably, small) resister R_V is included in *series* with the voltage source, which thus generates a finite current of $I = V_s/R_V$, instead of an infinite current, in the case of a short circuit across its terminals, and
- a (preferably, large) resister R_I is included in *parallel* with the current source, which thus generates a finite voltage of $V = I_s\,R_I$, instead of an infinite voltage, in the case of a open circuit across its terminals.

The current-voltage relationship of the practical voltage and current sources indicated in Figures 10.1e-f are given in Figure 10.2. Note that, taking $I_s = V_s/R_V$ and $R_I = R_V$, these two relationships are identical, and thus these two sources are, consistent with the following definition, said to be[11] "**equivalent**".

Fact 10.1 (Equivalent circuit definition) *Two circuits are said to be* **equivalent** *at a specified pair of terminals if they exhibit an identical current-voltage relationship, which may be static or dynamic.*

[10] Note that a **terminal** of an electric circuit or individual circuit element is a point at which other electric circuits are intended to be attached, as denoted by black dots in Figure 10.1.

[11] Though these two practical source models are "equivalent" from the perspective of the current-voltage relationship at their terminals, they are **not at all equivalent** in terms of their internal operation:

- a practical voltage source (e.g., a common battery) expends essentially no power whatsoever if there is an *open* circuit across its terminals (since the current through, and therefore the power consumed by, its internal resistor is zero in this case), but it expends significant power if there is a *short* circuit across its terminals (since the power consumed by its internal resistor in this case is $P = V_s\,I$, where $I = V_s/R_V$ for small R_V);

10.1.3.3 Sensors & actuators for interfacing with the physical world

To connect an electric circuit to the physical world, sensors and actuators[12] are needed, as surveyed in §6. Actuators are often built from some type of **electric motor** (see §6.8-6.11); others include **linear actuators** (like **voice coils**), **electroactive polymers**, etc. Common sensors include **accelerometers** (**accels**) to measure linear acceleration, **gyroscopes** (**gyros**) to measure angular acceleration, **encoders** to measure wheel rotation, **thermocouples** to measure temperature, etc. Note that some actuators which convert electrical energy to mechanical energy (like motors and piezoelectric actuators[13]) can also be used as sensors or **energy scavengers** to convert mechanical energy back into electrical energy (like generators and piezoelectric sensors[13]); this concept is central to the efficient operation of hybrid and fully electric cars, in which the motor normally used to drive the wheels may be operated as a generator during regenerative braking.

10.1.4 Kirchoff's laws

A **node** of an electric circuit is defined as any point at which two or more circuit elements (and, thus, two or more current paths) are connected. In a complex electric circuit with several circuit elements and several current paths, the following two simple rules facilitate analysis:

Fact 10.2 (Kirchoff's Current Law, or KCL) *The sum of the currents entering a node equals the sum of the currents leaving that node at any instant.*

Fact 10.3 (Kirchoff's Voltage Law, or KVL) *The sum of the voltages across the elements around any closed loop in a circuit is zero at any instant.*

Note that KVL may be satisfied *by construction*, simply by keeping track of the voltage at each *node* of the circuit, rather than the voltage drop across each circuit element. Note also that, in a circuit with n nodes, there are only $(n-1)$ independent KCL equations for the currents between these nodes, as the KCL at the last node may be derived by combining appropriately the KCL relations at the other $(n-1)$ nodes.

Defining the voltage at each node (thus implicitly satisfying the KVL equations) and the current between each node, writing KCL at all but one of the nodes, and writing the current-voltage relationship across each circuit element [see, e.g., (10.2a)-(10.2d)] leads to a set of ODEs which, together with the initial conditions, completely describe the time evolution of the circuit. This is best illustrated by a few examples.

Example 10.1 Voltage divider. Consider first a simple circuit formed as a series connection of two resistors, R_1 and R_2, with an ideal voltage source applied between the first node V_1 and the last node V_2, and denote by V_{mid} the voltage at the middle node. Since the current through the first resistor equals the current through the second resistor by KCL, applying (10.2a) leads immediately to

$$I_1 = I_2 \quad \Rightarrow \quad \frac{V_1 - V_{\text{mid}}}{R_1} = \frac{V_{\text{mid}} - V_2}{R_2} \quad \Rightarrow \quad V_{\text{mid}} = \frac{R_2\, V_1 + R_1\, V_2}{R_1 + R_2}.$$

It is seen that $V_{\text{mid}} = (V_1 + V_2)/2$ if $R_1 = R_2$, that $V_{\text{mid}} \to V_1$ if $R_1 \ll R_2$, and that $V_{\text{mid}} \to V_2$ if $R_2 \ll R_1$. $\triangle$

- in contrast, a practical current source (e.g., as developed in Examples 10.15 and 10.16) expends essentially no power whatsoever if there is a *short* circuit across its terminals (since the voltage across, and therefore the power consumed by, its internal resistor is zero in this case), but it expends significant power if there is an *open* circuit across its terminals (since the power consumed by its internal resistor in this case is $P = V\, I_s$, where $V = I_s\, R_I$ for large R_I).

[12] More broadly, devices which convert one form of energy (electric, mechanical, thermal, etc.) to another are called **transducers**.

[13] That is, actuators/sensors built on materials exhibiting the **piezoelectric effect**, generating an electric field in response to applied mechanical strain, and the **reverse piezoelectric effect**, generating mechanical strain in response to an applied electric field.

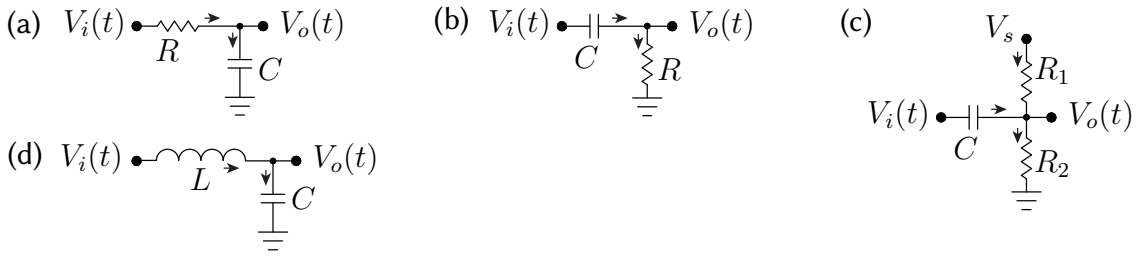


Figure 10.3: Four simple passive filters: (a) a first-order low-pass RC filter, (b) a first-order high-pass RC filter, (c) a voltage-biased first-order high-pass RC filter, and (d) a second-order low-pass LC filter.

Example 10.2 Passive filters. Consider now the four circuits shown in Figures 10.3a-c, and assume that

(a) the input voltage $V_i(t)$ is precisely specified regardless of the current drawn by the filter, and
(b) the current, if any, out the output terminal [marked $V_o(t)$ in the figure] is negligible.

It follows (see code in RR Chapter 10) that the **first-order low-pass RC filter** in Figure 10.3a is governed by

$$I_R = I_C, \quad V_i - V_o = I_R\,R, \quad I_C = C\,\frac{d\,V_o}{dt} \quad \Rightarrow \quad V_i(s) - V_o(s) = R\,C\,s\,V_o(s) \quad \Rightarrow \quad \frac{V_o(s)}{V_i(s)} = \frac{\omega_1}{s+\omega_1}$$

where $\omega_1 = 1/(R\,C)$, the **first-order high-pass RC filter** in Figure 10.3b is governed by

$$I_C = I_R, \quad I_C = C\,\frac{d[V_i - V_o]}{dt}, \quad V_o = I_R\,R \quad \Rightarrow \quad R\,C\,s\,[V_i(s) - V_o(s)] = V_o(s) \quad \Rightarrow \quad \frac{V_o(s)}{V_i(s)} = \frac{s}{s+\omega_1},$$

the **voltage-biased first-order high-pass RC filter** in Figure 10.3c is governed by

$$I_C + I_1 = I_2, \quad I_C = C\,\frac{d[V_i - V_o]}{dt}, \quad (V_s - V_o) = I_1\,R_1, \quad V_o = I_2\,R_2 \quad \Rightarrow$$

$$V_o(s) = \frac{R_2\,V_s}{R_1 + R_2 + R_1\,R_2\,C\,s} + \frac{R_1\,R_2\,C\,s\,V_i(s)}{R_1 + R_2 + R_1\,R_2\,C\,s} = \frac{R_2}{R_1+R_2}\,\frac{\omega_2}{s+\omega_2}\,V_s + \frac{s}{s+\omega_2}\,V_i(s)$$

where the effective resistance R_e is $R_e = R_1 R_2/(R_1 + R_2)$ [that is, $1/R_e = 1/R_1 + 1/R_2$] and $\omega_2 = 1/(R_e\,C)$, and the **second-order low-pass LC filter** in Figure 10.3d is governed by

$$I_L = I_C, \quad V_i - V_o = L\,\frac{d[I_L]}{dt}, \quad I_C = C\,\frac{d\,V_o}{dt} \quad \Rightarrow \quad V_i(s) - V_o(s) = L\,C\,s^2\,V_o(s) \quad \Rightarrow \quad \frac{V_o(s)}{V_i(s)} = \frac{\omega_3^2}{s^2+\omega_3^2}$$

where $\omega_3 = 1/\sqrt{L\,C}$. Assumptions (a) and (b) above are quite restrictive, however: if the inputs of such **passive filters** are attached to real sensors, if they are cascaded, or if their outputs are attached to real actuators, one or both of these assumptions are generally invalid. To tune the dynamic behavior of a filter circuit precisely even when assumptions (a) and (b) are relaxed, we thus need **active filters**, as developed in §10.2.

Nevertheless, the simple low-pass and high-pass filters illustrated in Figure 10.3 are useful building blocks for the circuits developed in the remainder of this chapter. As noted in §10.1.3, when excited by a sinusoid (or, by a square wave, which amounts to a sum of sinusoids), the power absorbed by an ideal inductor or capacitor, averaged over a multiple of periods $T = 2\pi/\omega$, is exactly zero. Thus, in sharp contrast with resistors (which always dissipates power), both inductors and capacitors act like "springs" of sorts, just storing and releasing energy when excited sinusoidally (see Footnote 6 on page 10-4, noting that real inductors and capacitors actually also have a bit of resistance). LC second-order low-pass filters in particular thus operate with very high energetic efficiency, even though their precise dynamic behavior depends on the load applied when assumptions (a) and/or (b) are relaxed. Indeed, when looking at a circuit board of a computer or cyber-physical system, the only place that you will commonly see inductors being used is as low-pass filters in the power regulation circuitry; elsewhere, resistors and capacitors (which are smaller and cheaper) are generally used instead. △

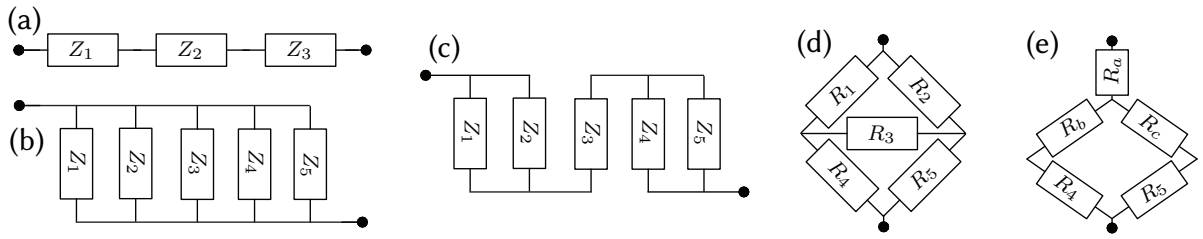


Figure 10.4: (a) Series, (b) parallel, and (c) "reducible" networks of a single type of component, with the Z_k denoting either resistors R_k, capacitors C_k, or inductors L_k; (d) a so-called "irreducible" network of resistors, and (e) an equivalent "reducible" network of resistors, with $\{R_a, R_b, R_c\}$ given by (10.3a).

Example 10.3 Equivalent resistance, capacitance, and inductance. The notion of equivalent circuits, with identical current-voltage relationships at one or more pairs of terminals, was defined in Fact 10.1. By the KCL and KVL, it follows that a set of n resistors, capacitors, or inductors in a **series connection** (see Figure 10.4a), in which the current I through the devices is equal and the voltages add[14], $\Delta V_1 + \Delta V_2 + \ldots \Delta V_n = \Delta V$, have the **equivalent resistance** R, **equivalent capacitance** C, or **equivalent inductance** L, respectively, of:

$$\begin{array}{lllll}
\Delta V_1 = I\,R_1, & \Delta V_2 = I\,R_2, & \ldots & \Delta V_n = I\,R_n & \Rightarrow \quad \Delta V = I\,R \quad \text{where} \quad R = R_1 + R_2 + \ldots R_n, \\
\dfrac{d\,\Delta V_1}{dt} = \dfrac{I}{C_1}, & \dfrac{d\,\Delta V_2}{dt} = \dfrac{I}{C_2}, & \ldots & \dfrac{d\,\Delta V_n}{dt} = \dfrac{I}{C_n} & \Rightarrow \quad \dfrac{d\,\Delta V}{dt} = \dfrac{I}{C} \quad \text{where} \quad \dfrac{1}{C} = \dfrac{1}{C_1} + \dfrac{1}{C_2} + \ldots \dfrac{1}{C_n}, \\
\Delta V_1 = L_1 \dfrac{dI}{dt}, & \Delta V_2 = L_2 \dfrac{dI}{dt}, & \ldots & \Delta V_n = L_n \dfrac{dI}{dt} & \Rightarrow \quad \Delta V = L\,\dfrac{dI}{dt} \quad \text{where} \quad L = L_1 + L_2 + \ldots L_n.
\end{array}$$

Similarly, a set of n resistors, capacitors, or inductors in a **parallel connection** (see Figure 10.4b), in which the voltage ΔV across the devices is equal and the currents add, $I_1 + I_2 + \ldots I_n = I$, have the **equivalent resistance** R, **equivalent capacitance** C, or **equivalent inductance** L, respectively, of:

$$\begin{array}{lllll}
I_1 = \dfrac{\Delta V}{R_1}, & I_2 = \dfrac{\Delta V}{R_2}, & \ldots & I_n = \dfrac{\Delta V}{R_n} & \Rightarrow \quad I = \dfrac{\Delta V}{R} \quad \text{where} \quad \dfrac{1}{R} = \dfrac{1}{R_1} + \dfrac{1}{R_2} + \ldots \dfrac{1}{R_n}, \\
I_1 = C_1 \dfrac{d\,\Delta V}{dt}, & I_2 = C_2 \dfrac{d\,\Delta V}{dt}, & \ldots & I_n = C_n \dfrac{d\,\Delta V}{dt} & \Rightarrow \quad I = C\,\dfrac{d\,\Delta V}{dt} \quad \text{where} \quad C = C_1 + C_2 + \ldots C_n, \\
\dfrac{dI_1}{dt} = \dfrac{\Delta V}{L_1}, & \dfrac{dI_2}{dt} = \dfrac{\Delta V}{L_2}, & \ldots & \dfrac{dI_n}{dt} = \dfrac{\Delta V}{L_n} & \Rightarrow \quad \dfrac{dI}{dt} = \dfrac{\Delta V}{L} \quad \text{where} \quad \dfrac{1}{L} = \dfrac{1}{L_1} + \dfrac{1}{L_2} + \ldots \dfrac{1}{L_n}.
\end{array}$$

In "reducible" networks of a single type of components, repeated application of the above simple rules for series and parallel connections of a single type of components is sufficient to determine an equivalent single component value. For example, if the Z_k in Figure 10.4c denote resistors, then

- the equivalent resistance of the parallel connection of R_1 and R_2 is $R_a = R_1 R_2/(R_1 + R_2)$,
- the equivalent resistance of the parallel connection of R_4 and R_5 is $R_b = R_4 R_5/(R_4 + R_5)$, and
- the equivalent resistance of the entire series connection (of R_a, R_3, and R_b) is $R = R_a + R_3 + R_b$.

On the other hand, repeated application of the above rules for parallel and series connections of a single type of components is not sufficient to simplify a so-called "irreducible" network, such as that shown in Figure 10.4d, to an equivalent single component value. However, repeated appliction of the Y-Δ transformation discussed in Example 10.4 below can often convert such a network to a reducible form, as shown in Figure 10.4e. $\triangle$

[14] In order to apply KVL as stated, visualize a battery connected across the terminals in each of the circuits in Figure 10.4.

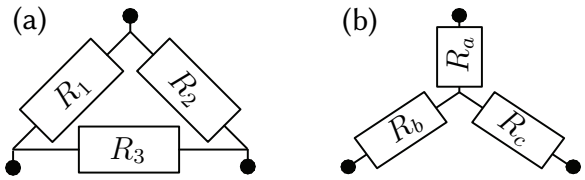


Figure 10.5: Two electrical networks with equivalent voltage/current relationships between their three nodes.

Example 10.4 The **Y-Δ transformation** is an analysis technique for electrical networks based on the equivalent resistance between any two nodes of two different appropriately-configured resistor networks, one shaped like a Y (upside down, sorry) and one shaped like a Δ, as shown in Figure 10.5. The relations between the resistors of the Δ network and those of the Y network that achieves this equivalence may easily be worked out in Matlab (see code in RR Chapter 10), which results in

$$R_a = \frac{R_1\,R_2}{R_1+R_2+R_3}, \qquad R_b = \frac{R_1\,R_3}{R_1+R_2+R_3}, \qquad R_c = \frac{R_2\,R_3}{R_1+R_2+R_3}, \tag{10.3a}$$

$$R_1 = \frac{R_a\,R_b + R_a\,R_c + R_b\,R_c}{R_c}, \quad R_2 = \frac{R_a\,R_b + R_a\,R_c + R_b\,R_c}{R_b}, \quad R_3 = \frac{R_a\,R_b + R_a\,R_c + R_b\,R_c}{R_a}; \tag{10.3b}$$

the relations in (10.3a) may be used to determine $\{R_a, R_b, R_c\}$ from $\{R_1, R_2, R_3\}$, and the relations in (10.3b) may be used to determine $\{R_1, R_2, R_3\}$ from $\{R_a, R_b, R_c\}$.

This equivalence may be used, e.g., to convert the "irreducible" network of resistors in Figure 10.4d into the "reducible" network in Figure 10.4e, with $\{R_a, R_b, R_c\}$ as given in (10.3a), thus upon simplification giving the equivalent resistance R of the entire network in Figure 10.4d as

$$\begin{aligned} R &= R_a + 1/[1/(R_b+R_4) + 1/(R_c+R_5)] = \ldots \\ &= \frac{R_1R_2R_3 + R_1R_2R_4 + R_1R_2R_5 + R_1R_3R_5 + R_2R_3R_4 + R_1R_4R_5 + R_2R_4R_5 + R_3R_4R_5}{R_1R_3 + R_1R_4 + R_2R_3 + R_1R_5 + R_2R_4 + R_2R_5 + R_3R_4 + R_3R_5}. \end{aligned} \qquad \triangle$$

To save significant time at this level (post high school), and to *entirely prevent* algebra mistakes, we may (and, indeed, should!) use **symbolic manipulation** everywhere possible to perform simple algebraic manipulations of systems of equations. We illustrate in RR Chapter 10 two distinct ways of doing this[15].

One way, as illustrated in the codes associated with, e.g., Examples 10.4 and 10.11, is to list the equations to be solved in a symbolic algebraic form that is easy to read, then to call a sophisticated solver that performs a series of substitutions and rearrangements in order to solve these n equations in the n unknowns specified. Note that this approach works for both linear and (significantly) even certain nonlinear equations.

The other way, illustrated in the codes associated with, e.g., Examples 10.1, 10.2, 10.5, 10.6, 10.10, and 10.12, is designed specifically for linear systems of equations. It first incorporates the n equations to be solved (in n unknowns) as Ax=b, then calls a symbolic version of Gaussian elimination (see §2.2 of *NR*) to compute the solution x given A and b. Note in particular, in the several examples provided, that well-structured comments in the vicinity of the lines of code that define A and b significantly improve readability, minimizing transcription errors. One of the benefits of this approach is that it is readily apparent under what conditions the set of equations being combined cease to be independent from each other, and thus the matrix A becomes singular, which can be monitored by keeping an eye on the **condition number** (see §2.5 of *NR*) of A.

[15] Of course, following the recommendations of Appendix A, make certain that you comment your codes sufficiently (in English, please!) to make such codes easy to understand and debug.

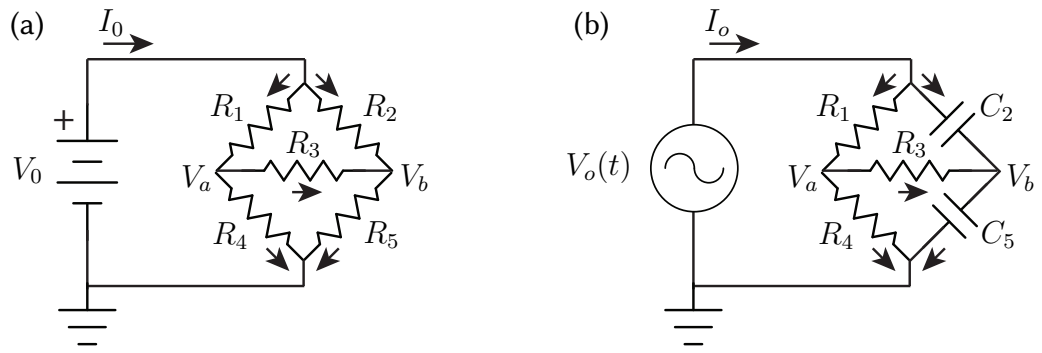


Figure 10.6: Wheatstone bridges for accurate measurement of (a) resistance, and (b) capacitance.

Example 10.5 Full analysis of a Wheatstone bridge. Consider the **Wheatstone bridge** of Figure 10.6a. For convenience, we number the elements of a circuit sequentially, and denote by I_k the current through element k, with positive current indicated by the direction of the arrow (this keeps us from having to label each current component individually in the figure). The (constant) voltage at the top of the bridge is V_0 (as it is connected to the top of the battery), and the voltage at the bottom of the bridge is 0 (as it is connected to the bottom of the battery, which is defined as ground), thus leaving two undetermined nodal voltages, $\{V_a, V_b\}$. We may thus determine the eight unknowns $\{I_0, I_1, I_2, I_3, I_4, I_5, V_a, V_b\}$ given the six parameters $\{V_0, R_1, R_2, R_3, R_4, R_5\}$ via KCL at three of the four nodes and the current-voltage relationship across each of the five resistors:

$$I_0 = I_1 + I_2, \quad I_1 = I_3 + I_4, \quad I_2 + I_3 = I_5, \tag{10.4a}$$

$$V_o - V_a = I_1 R_1, \quad V_o - V_b = I_2 R_2, \quad V_a - V_b = I_3 R_3, \quad V_a = I_4 R_4, \quad V_b = I_5 R_5. \tag{10.4b}$$

These eight linear equations in the eight unknowns x={I0 , I1 , I2 , I3 , I4 , I5 , Va, Vb} may easily be written in the form Ax=b and solved for x, as illustrated in the corresponding code in RR Chapter 10, which is provided for $R_1 = R_2 = R_4 = 1\,\text{kohm}$, $R_3 = 100\,\text{kohm}$, and $V_0 = 5\,\text{V}$, keeping R_5 as symbolic (all choices that are easily changed), from which it follows immediately that $I_3 = (1000 - R_5)/(4.06 \times 10^4\, R_5 + 4.02 \times 10^7)$ amps. Changing, e.g., to $R_1 = R_2 = 0$ in this algorithm shows how the resulting system of equations can become singular.

The Wheatstone bridge is particularly useful for the precise measurement of an unknown resistor value (taken here as R_5) given three accurately known (often, equal) resister values (taken here as $\{R_1, R_2, R_4\}$), and a center resistor R_3. Indeed, if $R_1/R_4 = R_2/R_5$, then the bridge is said to be **balanced**, and the current through the resister in the center of the bridge, I_3 (which may be measured precisely using a **galvanometer**), will be exactly zero, as $V_a = V_b$ in this case. △

Example 10.6 A Wheatstone bridge for measuring capacitance. If we simply replace the resistors R_2 and R_5 in Figure 10.6a with capacitors C_2 and C_5, where C_2 is known and C_5 is unknown, and observe the circuit at steady state, we run into a problem: setting the time derivatives of the current through the capacitors equal to zero (that is, taking $I_2 = I_5 = 0$), it follows that $I_3 = 0$ and thus $V_a = V_b$ regardless of the value of C_5! Thus, C_5 can *not* be determined in this simplistic manner.

However, as indicated in Figure 10.6b, if we replace resistors R_2 and R_5 with capacitors C_2 and C_5, and we also replace the constant voltage source with a (sinusoidal) time-varying voltage source, then we can now easily determine C_5. Our eight equations for the eight unknowns $\{I_0, I_1, I_2, I_3, I_4, I_5, V_a, V_b\}$ now take the form

$$I_0 = I_1 + I_2, \quad I_1 = I_3 + I_4, \quad I_2 + I_3 = I_5,$$

$$V_o - V_a = I_1 R_1, \quad I_2 = C_2\, d(V_o - V_b)/dt, \quad V_a - V_b = I_3 R_3, \quad V_a = I_4 R_4, \quad I_5 = C_5\, d(V_b)/dt,$$

where only the equations in blue have changed. Assuming $R_1 = R_2 = 1\,\text{k}\Omega$, $C_3 = 10\,\mu\text{F}$, and $R_5 = 100\,\text{k}\Omega$, that $\{I_0, I_1, I_2, I_3, I_4, I_5, V_a, V_b, V_o\}$ are all initially zero, taking the Laplace transform [see §10.1.5], and performing

an analogous symbolic manipulation, as shown in the corresponding Wheatstone capacitors code in RR Chapter 10, it follows that, in Laplace transform space,

$$\frac{I_3(s)}{V_0(s)} = G(s) = \frac{(C_5 - C_2)s}{2.01 \times 10^5 (C_5 + C_2)s + 2}.$$

As in the case of drawing Bode plots (see §9.4.1), we are interested in the magnitude and phase of the persistent sinusoidal component of the output current $I_3(t)$ when the input voltage $V_0(t)$ is sinusoidal. That is, for the transfer function $G(s)$ given above, taking $V_0(t) = V\sin(\omega t)$ will result in $I_3(t) = I\sin(\omega t + \phi)+$ terms that decay with time, where $I = |G(\mathrm{i}\omega)|$ and $\phi = \angle G(\mathrm{i}\omega)$, and thus

$$\frac{I}{V} = \frac{|C_5 - C_2|\,\omega}{\sqrt{[2.01 \times 10^5 (C_5 + C_2)]^2\omega^2 + 4}}, \quad \phi = \begin{cases} 90° - \text{atan2}\{[2.01 \times 10^5 (C_5 + C_2)]\omega, 2\} & \text{if } C_5 > C_2, \\ -90° - \text{atan2}\{[2.01 \times 10^5 (C_5 + C_2)]\omega, 2\} & \text{if } C_5 < C_2. \end{cases}$$

If $\omega = 0$, then $I = 0$ regardless of C_5, consistent with the comments made in the previous paragraph.
If $\omega > 0$ and $I = 0$, it follows immediately that the bridge is in balance, and thus $C_5 = C_2 = 10\ \mu$F.
If $\omega > 0$ and $I \neq 0$, C_5 may be determined from I according to the above expressions (with $C_5 > C_2$ if $\phi > 0$, and $C_5 < C_2$ if $\phi < 0$; note the $180°$ phase shift in ϕ when C_5 is changed from below C_2 to above C_2).

Inductance may be quantified with a Wheatstone bridge in an analogous fashion (see Exercise 10.2). △

Example 10.7 Equivalent sources Any combination of voltage sources, current sources, and resistors leads to a linear current-voltage relationship like those in Figure 10.2; the following facts follow as consequence.

Fact 10.4 (Thévenin's theorem) *Any circuit containing only voltage sources, current sources, and resistors can be converted to a* **Thévenin equivalent circuit***, with one ideal voltage source and one resistor in series.*

Fact 10.5 (Norton's theorem) *Any circuit containing only voltage sources, current sources, and resistors can be converted to a* **Norton equivalent circuit***, with one ideal current source and one resistor in parallel.*

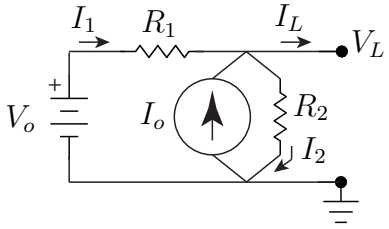


Figure 10.7: A circuit with both voltage and current sources as well as two resistors.

To illustrate, consider the circuit shown in Figure 10.7. Writing down KCL at the node at the top of the circuit and Ohm's law across each resistor, the (linear) current-voltage relationship at the terminals may be determined:

$$\left.\begin{aligned} I_1 + I_o &= I_L + I_2 \\ V_o - V_L &= I_1 R_1 \\ V_L &= I_2 R_2 \end{aligned}\right\} \quad \Rightarrow \quad I_L = I_o + I_1 - I_2 = \left(I_o + \frac{V_o}{R_1}\right) - \left(\frac{1}{R_1} + \frac{1}{R_2}\right)V_L. \tag{10.5}$$

It follows from this analysis of the circuit in Figure 10.7 that

- its Thévenin equivalent (Figure 10.1e) sets $R_V = R_1 R_2/(R_1 + R_2)$ and $V_s = (I_o + V_o/R_1)R_V$, and
- its Norton equivalent (Figure 10.1f) sets $R_I = R_1 R_2/(R_1 + R_2)$ and $I_s = I_o + V_o/R_1$;

note that all of these circuits have identical current-voltage relationships, as illustrated in Figure 10.2.

Of particular interest in this example is the question of how much power is actually provided by the two sources in Figure 10.7. To simplify, assume first that $R_1 = I_L = 0$; in this case, $V_L = V_o$, and

- the power absorbed by the current source is $-I_o V_o < 0$ (that is, power is *provided* by the current source regardless of the relative magnitudes of I_o and V_o/R_2), whereas
- the power absorbed by the voltage source is $-I_1 V_o = -(I_2 - I_o)V_o = -(V_o/R_2 - I_o)V_o$ (that is, power is *provided* by the voltage source if $V_o/R_2 > I_o$, and is *absorbed* by the voltage source if $V_o/R_2 < I_o$).

Taking $R_1 > 0$ and $I_L \neq 0$, similar conclusions may be drawn (see Exercise 10.3). △

10.1.5 Laplace transform analysis of circuits and the definition of impedance

In simple circuits without capacitors or inductors, combining KCL and the current-voltage relationship across each component leads to straightforward systems of *linear algebraic equations*, which may be solved by hand or with symbolic numerical tools. In more interesting circuits incorporating capacitors and/or inductors, combining KCL and the current-voltage relationship across each component often leads, more generally, to sets of *linear constant-coefficient ODEs* together with various algebraic constraints (jointly referred to as **descriptor systems**). Without the Laplace transform, as developed in §9, the analysis of such systems would be difficult. However, as seen in the various examples presented above, application of the Laplace transform to such systems converts them back to straightforward systems of algebraic equations, incorporating the Laplace transform variable s, that are again easy to solve by hand or with simple symbolic numerical tools.

It is thus seen that, when analyzing electric circuits, *working in the Laplace domain is essential*. Further, one is often interested in the *frequency response* of an electric circuit subject to sinusoidal excitation. As shown in §9.4.1, the gain and phase shift of the persistent sinusoidal component of the output of a linear system $G(s)$ when excited by a sinusoidal input may be summarized by the Bode plot of $G(s)$, and may be calculated simply by evaluating the magnitude and phase of $G(\mathrm{i}\,\omega)$ as a function of the frequency ω of the input sinusoid.

Example 10.8 Impedance of the fundamental circuit elements. Taking the Laplace transform of the current-voltage relationships of resistors, capacitors, and inductors [see (10.2)] and evaluating at $s = \mathrm{i}\,\omega$ gives

$$G_{\text{resistor}}(\mathrm{i}\omega) = \frac{V(\mathrm{i}\omega)}{I(\mathrm{i}\omega)} = R \triangleq Z_R, \quad G_{\text{capacitor}}(\mathrm{i}\omega) = \frac{V(\mathrm{i}\omega)}{I(\mathrm{i}\omega)} = \frac{-\mathrm{i}}{\omega\, C} \triangleq Z_C, \quad G_{\text{inductor}}(\mathrm{i}\omega) = \frac{V(\mathrm{i}\omega)}{I(\mathrm{i}\omega)} = \mathrm{i}\,\omega\, L \triangleq Z_L.$$

The quantities Z_R, Z_C, and Z_L are used often, and are commonly referred as the **impedance** of each of these components. In other texts, the concept of impedance is often discussed somewhat loosely as a *complex, frequency-dependent generalization of resistance* even before Laplace transforms are properly introduced. This approach is, perhaps, unnecessarily convoluted; pedagogically, the author recommends instead mastering the Laplace transform (§9.2) and Bode plot (§9.4.1) *before* reading the present discussion (and that which follows); the frequency response of the current-voltage relationships represented by the (complex) transfer functions $G_{\text{resistor}}(s)$, $G_{\text{capacitor}}(s)$, and $G_{\text{inductor}}(s)$ as listed above [and, $G_{\text{speaker}}(s)$ and $G_{\text{piezo}}(s)$, as discussed in Examples 10.9 and 10.10 below] are then quite easy to interpret. In particular, these characterizations are consistent with the phenomenological description of the general behavior of capacitors and inductors given in §10.1.3.1:

- the voltage across a capacitor *lags* the current through the capacitor by 1/4 cycle [$\phi = -90°$, associated with the $-\mathrm{i}$ factor in $G_{\text{capacitor}}(\mathrm{i}\,\omega)$], with the magnitude of the sinusoidal voltage across the capacitor divided by the magnitude of the sinusoidal current through the capacitor *decreasing* with frequency ω;
- the voltage across an inductor *leads* the current through the inductor by 1/4 cycle [$\phi = 90°$, associated with the i factor in $G_{\text{inductor}}(\mathrm{i}\,\omega)$], with the magnitude of the sinusoidal voltage across the inductor divided by the magnitude of the sinusoidal current through the inductor *increasing* with frequency ω. △

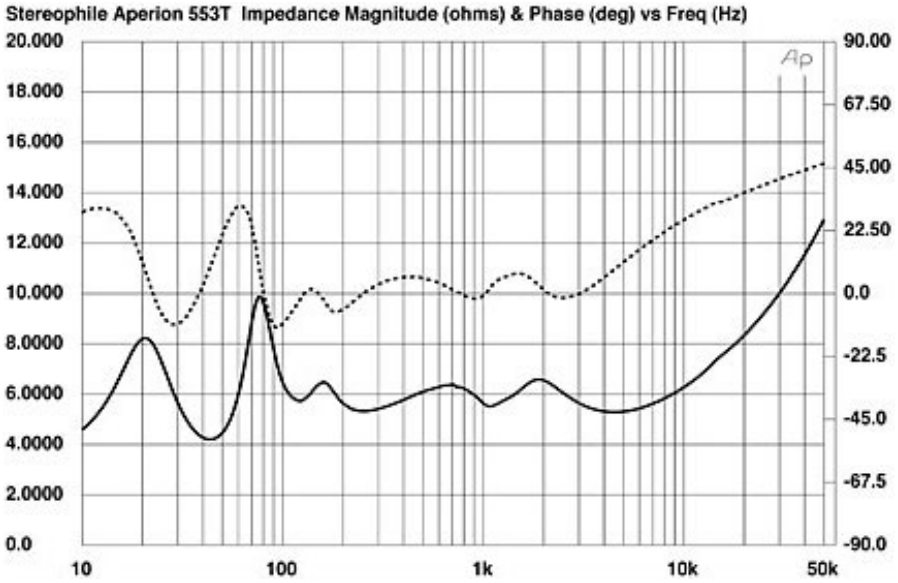


Figure 10.8: Bode plot of the transfer function $G(s) = V(\mathrm{i}\,\omega)/I(\mathrm{i}\,\omega)$ from current to voltage, also referred to as the **impedance**, of a Aperion Audio Intimus 533-T loudspeaker. The horizontal axis is the log of the frequency in Hz (not rad/s, which is typical in controls). The solid curve indicates the magnitude, with its (linear) scale at left; note the magnitude is around 6 ohms (varying between about 5.3 ohms and 6.7 ohms) over audio frequencies from 100 Hz to 10 kHz. The dotted curve indicates the phase, with scale at right in units of degrees; note the phase is around 0° (varying between about -10° and 23°) over audio frequencies from 100 Hz to 10 kHz. Plot courtesy of Stereophile.com.

Example 10.9 Impedance of an audio speaker. Figure 10.8a illustrates the Bode plot of the transfer function $G_{\text{speaker}}(s) = V(s)/I(s)$, from current to voltage, of a typical audio speaker. This plot is commonly referred to as the (frequency-dependent) **impedance** of the speaker. If this device presented a purely resistive load to the electric circuit, the magnitude of the impedance (measured in ohms; 4 ohm, 6 ohm, and 8 ohm speakers are common) would be constant across all frequencies, and its phase would be zero. However, a speaker is of course *not* a simple resistive load; rather, its Bode plot depends on the mechanical and electrical details of its construction. Nevertheless, over typical audio frequencies (from 100 Hz to 10 kHz), it is seen that this speaker approximates a simple resistive load of around 6 ohm. Looking a bit more closely, the magnitude part of this Bode plot, $|G(\mathrm{i}\,\omega)|$, reveals peaks and valleys ("resonances" and "antiresonances") as a function of frequency, and the phase part of this Bode plot is generally somewhat positive wherever $|G(\mathrm{i}\,\omega)|$ is increasing with ω, and somewhat negative wherever $|G(\mathrm{i}\,\omega)|$ decreases with with ω. △

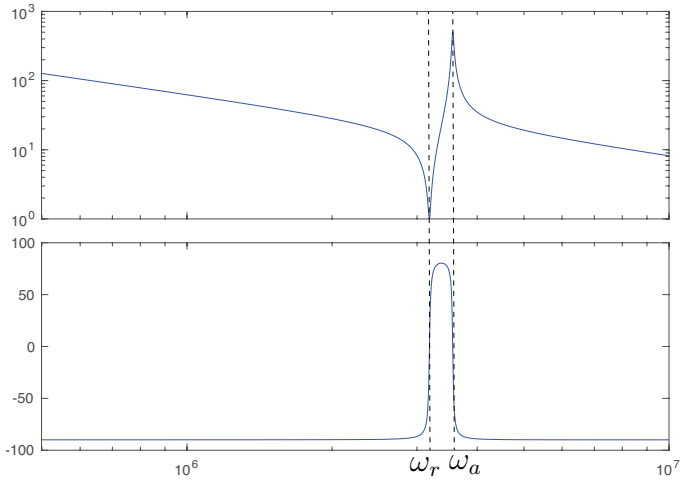


Figure 10.9: Bode plot of the transfer function $G(s) = V(\mathrm{i}\,\omega)/I(\mathrm{i}\,\omega)$ from current to voltage, also referred to as the **impedance**, of the Butterworth/van Dyke circuit model of a piezoelectric material. The system is said to be essentially **inductive** ($\phi \approx 90°$) for $\omega_r < \omega < \omega_a$, and essentially **capacitive** ($\phi \approx -90°$) outside this range.

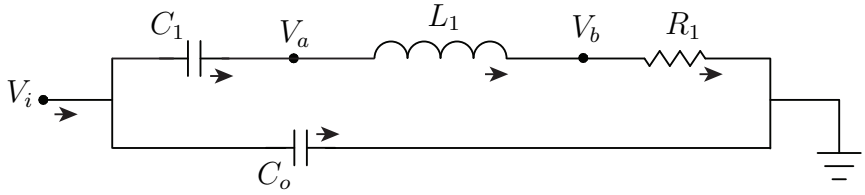


Figure 10.10: The Butterworth/van Dyke circuit model of a piezoelectric material, as considered in Example 10.10.

Example 10.10 Impedance of piezos. Many crystalline materials, such as quartz crystals, exhibit a **piezoelectric effect** such that

- when a voltage is applied across the material, it mechanically deforms, and
- when the material is deformed, a charge accumulates on its surface that generates a measurable voltage.

Electromechanical devices (both sensors and actuators) that exhibit strong resonant oscillations may be constructed using such piezoelectric materials. A model electric circuit capturing the essence of such electromechanical devices is illustrated in Figure 10.10. The (Laplace-transformed) equations governing this circuit are

$$I_i = I_o + I_1, \quad I_o = C_o\, s\, V_i, \quad I_1 = C_1\, s\, [V_i - V_a], \quad [V_a - V_b] = s\, L_1\, I_1, \quad V_b = R_1\, I_1;$$

that is, 5 eqns in the 5 variables $\mathbf{x}(s) = \{I_o(s), I_1(s), V_i(s), V_a(s), V_b(s)\}$, treating the current $I_i(s)$ as an input and $\{C_o, C_1, L_1, R_1\}$ as parameters. Solving (see the corresponding code in RR Chapter 10) gives

$$G_{\text{piezo}}(s) = \frac{V_i(s)}{I_i(s)} = \frac{L_1\, C_1\, s^2 + R_1\, C_1\, s + 1}{s\,(L_1\, C_o\, C_1\, s^2 + R_1\, C_o\, C_1\, s + C_o + C_1)} = K \frac{s^2 + 2\,\zeta_r\,\omega_r\, s + \omega_r^2}{s(s^2 + 2\,\zeta_a\,\omega_a\, s + \omega_a^2)},$$

where $\omega_r = 1/\sqrt{L_1\, C_1}$, $\zeta_r = R_1/(2\,\omega_r\, L_1)$, $\omega_a = 1/\sqrt{L_1\, C_a}$ with $C_a = C_o\, C_1/(C_o + C_1)$, $\zeta_a = R_1/(2\,\omega_a\, L_1)$, $K = 1/C_o$; for $\{C_o, C_1, L_1, R_1\} = \{2\,\text{nF}, 0.5\,\text{nF}, 5\,\mu\text{H}, 1\,\text{ohm}\}$, the Bode plot of $G_{\text{piezo}}(s)$ is given in Figure 10.8b, indicating a lightly-damped resonance and antiresonance at $\omega_r = 3.18\,\text{MHz}$ and $\omega_a = 3.56\,\text{MHz}$. △

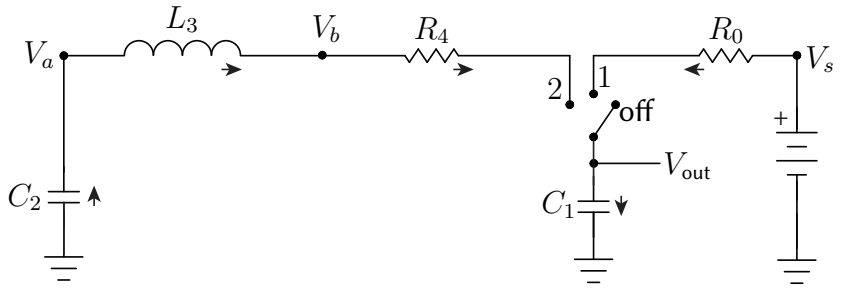


Figure 10.11: The **LC tank oscillator** considered in Example 10.11.

Example 10.11 LC tank oscillator. We now consider the oscillator circuit in Figure 10.11, initialized with the switch in the **off** position, current equal to zero everywhere, and all capacitors fully discharged.

Startup. At $t = 0$, with $V_{\text{out}}(t=0) = 0$, we turn the switch from off to **position 1**. Current flows from the battery, at voltage V_s, through R_0, through C_1, to ground. Denoting the current through component i as $I_i(t)$, with positive current in the direction of the arrows shown, KCL and the component equations for R_0 and C_1 are

$$I_0(s) = I_1(s), \quad V_s - V_{\text{out}}(s) = R_0\, I_0(s), \quad s\, C_1 V_{\text{out}}(s) = I_1(s).$$

These three eqns in $\{I_0(s), I_1(s), V_{\text{out}}(s)\}$ are easily reduced to one eqn in $V_{\text{out}}(s)$, and inverse transformed:

$$[V_s - V_{\text{out}}(s)]/R_0 = s\, C_1 V_{\text{out}}(s) \;\; \Rightarrow \;\; \boxed{(1 + R_0\, C_1 d/dt) V_{\text{out}}(t) = V_s, \;\; V_{\text{out}}(t=0) = 0}.$$

This inhomogeneous linear ODE has a homogeneous solution of $V_{\text{out}}(t) = A\, e^{-t/(R_0 C_1)}$ and a particular solution of $V_{\text{out}}(t) = V_s$. Summing these two solutions and matching the ICs (by taking $A = -V_s$) gives the full solution

$$V_{\text{out}}(t) = V_s(1 - e^{-t/(R_0 C_1)}). \tag{10.6a}$$

By the component equations for both R_0 and C_1, the corresponding current $I_0(t) = I_1(t) \triangleq I(t)$ is

$$I(t) = [V_s - V_{\text{out}}(t)]/R_0 = C_1\, dV_{\text{out}}(t)/dt \quad \Rightarrow \quad I(t) = (V_s/R_0)\, e^{-t/(R_0 C_1)}. \tag{10.6b}$$

The responses of $V_{\text{out}}(t)$ and $I(t)$ are characterized by exponential decay, with

$$V_{\text{out}}(t) \to V_s \quad \text{and} \quad I(t) \to 0 \quad \text{as} \quad t \to \infty. \tag{10.6c}$$

If you know values for $\{V_s, R_0, C_1\}$, the time t_s after which $V_{\text{out}}(t)$ settles to within, say, 95% of its steady state value is given by setting $0.95\, V_o = V_o(1 - e^{-t/(R_0 C_1)})$ and solving for t, giving

$$t = -R_0\, C_1 \ln(0.05) \approx 3\, R_0\, C_1. \tag{10.6d}$$

Decaying oscillations. Starting from the steady-state values of $V_{\text{out}}(t)$ and $I(t)$ determined in (10.6c), we now move the switch from position 1 to **position 2**. [For simplicity, we also reset the clock, so that $t = 0$ now corresponds to the time that we flip the switch to position 2.] KCL now gives

$$I_2(t) = I_3(t) = I_4(t) = I_1(t) \triangleq I(t). \tag{10.7}$$

Note also that the Laplace transform of $V'_{\text{out}}(t) = d[V_{\text{out}}(t)]/dt$ is $V'_{\text{out}}(s) = s\, V_{\text{out}}(s) - V_s$, due to its nonzero ICs.

Implementing KCL, given above, into the Laplace transform of the component equations for $\{C_1, C_2, L_3, R_4\}$, we have four eqns with three intermediate variables, $\{I(s), V_a(s), V_b(s)\}$, to be eliminated:

$$I(s) = s\, C_2\, [-V_a(s)], \quad V_a(s) - V_b(s) = s\, L_3\, I(s), \quad V_b(s) - V_{\text{out}}(s) = R_4 I(s), \quad I(s) = C_1[s\, V_{\text{out}}(s) - V_s].$$

Reducing these four algebraic eqns in the four variables $\{I(s), V_a(s), V_b(s), V_{\text{out}}(s)\}$ to one eqn in $V_{\text{out}}(s)$ is easily done by hand (or, better, in Matlab; see code in RR Chapter 10), giving immediately:

$$V_{\text{out}}(s) = \frac{b_2 s^2 + b_1 s + b_0}{s[s^2 + a_1 s + a_0]} \quad \text{with} \tag{10.8}$$
$$a_1 = \frac{R_4}{L_3}, \quad a_0 = \frac{1}{L_3 C}, \quad \frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} = \frac{C_1 + C_2}{C_1 C_2}, \quad b_2 = V_s, \quad b_1 = \frac{V_s R_4}{L_3}, \quad b_0 = \frac{V_s}{L_3 C_2}.$$

Noting the $e^{-\sigma t}\cos(\omega_d t)$ and $e^{-\sigma t}\sin(\omega_d t)$ entries in Table 9.1, and setting

$$s^2 + a_1 s + a_0 = (s+\sigma)^2 + \omega_d^2 = s^2 + 2\,\sigma\, s + (\sigma^2 + \omega_d^2) \quad \Rightarrow \quad \sigma = a_1/2, \quad \omega_d = \sqrt{a_0 - a_1^2/4},$$

we may rewrite (10.8) via partial faction expansion as

$$V_{\text{out}}(s) = \frac{b_2\, s^2 + b_1\, s + b_0}{s\,[(s+\sigma)^2 + \omega_d^2]} = B_2\,\frac{1}{s}\cdot\frac{(s+\sigma)^2 + \omega_d^2}{(s+\sigma)^2 + \omega_d^2} + B_1\frac{(s+\sigma)}{(s+\sigma)^2 + \omega_d^2}\cdot\frac{s}{s} + B_0\frac{\omega_d}{(s+\sigma)^2 + \omega_d^2}\cdot\frac{s}{s}. \tag{10.9}$$

This may be solved for $\{B_2, B_1, B_0\}$ by forming a common denominator, as shown above, and setting like powers of s in the numerator as equal (see corresponding code in RR Chapter 10), which immediately gives

$$B_2 = \frac{b_0}{\sigma^2 + \omega_d^2}, \quad B_1 = b_2 - B_2, \quad B_0 = \frac{b_1 - b_2\sigma}{\omega_d} - B_2\frac{\sigma}{\omega_d}.$$

Thus, for $t \geq 0$,

$$V_{\text{out}}(t) = B_2 + B_1\, e^{-\sigma t}\cos(\omega_d\, t) + B_0\, e^{-\sigma t}\sin(\omega_d\, t), \tag{10.10a}$$
$$I(t) = C_1 dV_{\text{out}}(t)/dt = C_1 e^{-\sigma t}[(-\sigma B_1 + \omega_d B_0)\,\cos(\omega_d\, t) + (-\sigma B_0 - \omega_d B_1)\,\sin(\omega_d\, t)], \tag{10.10b}$$

where the constants $\{\omega_d, \sigma, B_2, B_1, B_0\}$ depend on $\{V_s, R_0, C_1, C_2, L_3, R_4\}$ via the various equations above.

If $R_4 = 0$ and $C_1 = C_2$, then $C/C_1 = C/C_2 = 1/2$, $a_1 = b_1 = \sigma = B_0 = 0$, and $B_2 = B_1 = V_s/2$, and thus a sort of balanced "see-saw" effect sets in, with

$$V_{\text{out}}(t) = V_s[1 + \cos(\omega_d\, t)]/2, \qquad I(t) = -(C_1 V_s/2)\,\omega_d \sin(\omega_d\, t),$$
$$V_a(t) = V_{\text{out}}(t) + [L_3\, d/dt]I(t) = (V_s/2)[1 + \cos(\omega_d\, t) - L_3\, C_1\, \omega_d^2 \cos(\omega_d t)] = V_s[1 - \cos(\omega_d\, t)]/2];$$

that is, the charge shifts from C_1 to C_2 (i.e., from V_{out} to V_a), and back, sinusoidally (undamped) over the period

$$T = 2\pi/\omega_d = 2\pi\sqrt{L_3 C} \quad \Rightarrow \quad \boxed{T = 2\pi\sqrt{L_3 C_1 C_2/(C_1 + C_2)}.}$$

Again, there will always be some resistance in practical capacitors and inductors; we model its net effect in this circuit with the (small) resistor R_4. Any such resistance (e.g., taking $R_4 > 0$) will result in $\sigma > 0$, and thus cause the oscillations to decay in time. This decay may be offset with an op amp, as explored in Example 10.32. △

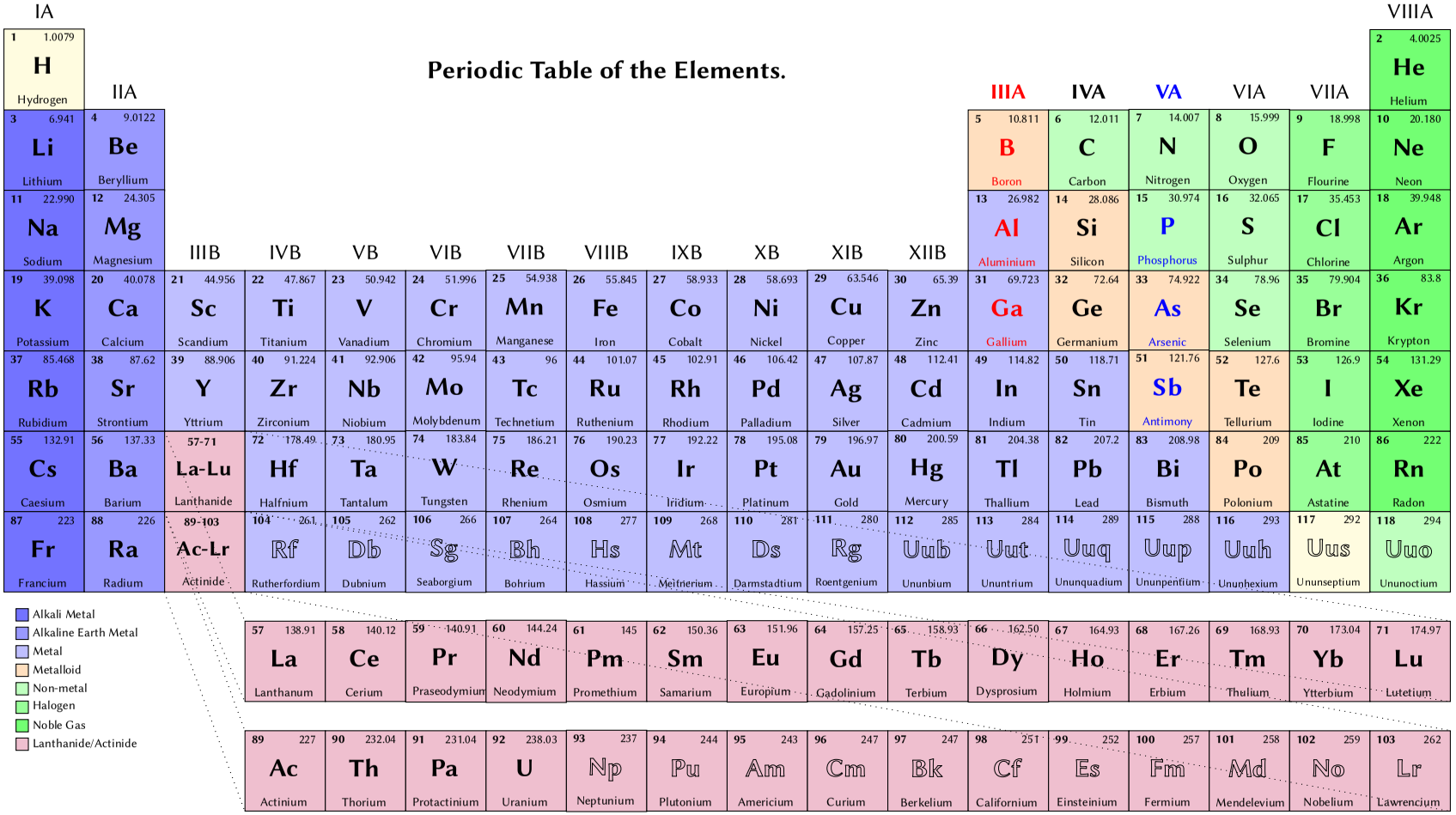


Figure 10.12: Periodic Table of the Elements, for providing context related to the structure of common semiconductors. Carbon, Silicon, and Germanium, which are all in column IVA (that is, the "carbon column"), crystallize in a **diamond crystal structure**. Gallium arsenide (equal parts Gallium, from column IIIA, and Arsenic, from column VA), crystallizes in a **zincblende crystal structure**, which is simply a diamond crystal structure with gallium and arsenic in alternating lattice sites. Silicon carbide can take any of about 250 crystalline forms, including zincblende. Note that **n-type dopants**, such as **phosphorus**, **arsenic**, or **antimony**, are taken from column VA (just to the right of the carbon column), thus introducing extra valence electrons (not bound by the crystal structure) that can move fairly easily when a voltage is applied. Similarly, **p-type dopants**, such as **boron**, **aluminum**, or **gallium**, are selected from column IIIA (just to the left of the carbon column), thuus introducing "holes" in the crystal's electron structure that can also move fairly easily when a voltage is applied.

10.2 Active analog circuits & filters

10.2.1 Semiconductor circuit elements

A **semiconductor** is a material (often, a single crystal[16]) that has conduction properties that may be tuned during fabrication in various useful ways. A single pure crystal of semiconductor material, such as silicon (see Figure 10.12), is generally nonconductive, as all of the **valence** (outer-shell) electrons of the constituent atoms are tied up by the **covalent bonds** of the crystal.

However, if a semiconductor crystal is formed, or **doped**, with **n-type dopant** atoms such as **phosphorus** (see Figure 10.12), an extra valence electron is introduced in the crystal lattice for each atom of the n-type dopant in the crystal. These extra valence electrons can move fairly easily when a voltage is applied across the material, thus making an n-doped semiconductor, such as phosphorus-doped silicon, a conductor.

Similarly, if a semiconductor crystal is formed with **p-type dopant** atoms such as **boron** (see Figure 10.12), a valence electron is missing from the crystal lattice for each atom of the p-type dopant present in the crystal, forming what is known as a "**hole**" in the electron structure of the crystal. These holes in the electron structure of the crystal can also move fairly easily[17] when a voltage is applied across the material, thus making a p-doped semiconductor, such as boron-doped silicon, also a conductor.

10.2.1.1 p-n junctions & diodes

When a semiconductor crystal has various neighboring sections, some that are p-doped and some that are n-doped, thus forming **p-n junctions** within the semiconductor, useful electrical characteristics arise. For example, a semiconductor crystal which has just two adjacent doped regions, with a single p-n junction in the middle, is called a **semiconductor diode**, which behaves in the ideal setting as follows:

- If a semiconductor diode is put under **forward bias**, with positive voltage applied to the p side of the semiconductor and negative voltage applied to the n side, then electrons will flow into the n side of the semiconductor, pushing free valence electrons in the crystal lattice towards the p-n junction. These electrons, in turn, flow into the nearby holes on the p side of the semiconductor and create, in effect, a flow holes on the p side of the semiconductor that is equal in magnitude and opposite in direction to the flow of electrons on the n side of the semiconductor, thus sustaining an electric current through the material with very little (ideally, zero) resistance[18].
- If a semiconductor diode is put under **reverse bias**, with positive voltage applied to the n side of the semiconductor and negative voltage applied to the p side, then some of the extra valence electrons on the n side of the semiconductor are pulled away from the p-n junction and out of the semiconductor, and some of the holes in the electron structure of the crystal on the p side of the semiconductor are pulled away from the p-n junction and, effectively, out of the semiconductor, creating a so-called **depletion layer** with neither holes nor free valence electrons to carry moving charge (that is, to sustain the current) in the vicinity of the p-n junction. As a result, an ideal diode under negative bias does not conduct.

[16] **Amorphous** semiconductors, which lack a long-range ordered crystal structure, can also be manufactured, and can be done so in especially thin layers over large areas. Such semiconductors may be doped in a manner similar to the single-crystal semiconductors discussed in §10.2.1, and can be switched from one physical state to another (e.g., from translucent to opaque), which makes them especially useful in a variety of applications, such as **CD**s/**DVD**s/**BD**s, **liquid-crystal displays** (**LCD**s), and **solar cells**.

[17] Note that it is actually a neighboring electron in the electron structure of a crystal lattice that moves, thereby changing the "hole" location in this electron structure; several successive movements of electrons into neighboring hole locations give the appearance that it is the hole itself that is moving.

[18] As a loose physical analogy of current flow in a diode under forward bias, one might visualize the electron motion (on the n-doped side) towards the p-n junction as tiny drops of rain falling through air toward an air/water interface, and the corresponding hole motion (on the p-doped side) towards the p-n junction as tiny bubbles of air rising through water toward the air/water interface at the same rate, resulting in zero net accumulation of negative or positive charge (raindrops or bubbles) at the interface.

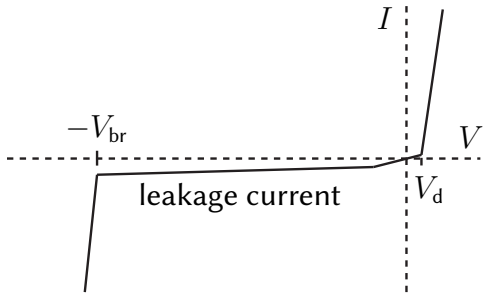


Figure 10.13: Typical current-voltage relationship of a real diode, with forward bias given by $V > 0$ and reverse bias given by $V < 0$, indicating the **breakdown voltage** V_{br}, the leakage current, and the **cut-in voltage** V_d.

Though the ideal model of a semiconductor diode described above is sometimes adequate, the deviations of real semiconductor diodes from this behavior, as indicated in Figure 10.13, are important to quantify:

- Within the depletion layer described above in the reverse bias setting, the n-doped side, now lacking its extra valence electrons, is positively charged, and the p-doped side, now lacking its holes, is negatively charged by the same amount. This sets up an electric field across the p-n junction. When the applied voltage exceeds a certain **breakdown threshold** V_{br} (typically 5 to 20 volts), one of two phenomena occurs (which phenomena sets in first depends on various particular details of the diode).
  - In **Zener breakdown**, this electric field directly breaks some of the covalent bonds in the semiconductor crystal, thus allowing the resulting freed electrons to act as charge carriers.
  - In **avalanche breakdown**, on the other hand, the electric field accelerates free valence electrons near the edge of the depletion layer to sufficient energies that their subsequent collision with bound electrons can break covalent bonds within the depletion layer, resulting in the creation of additional charge carriers (pairs of free electrons and holes), which in turn collide with other bound electrons within the depletion layer to create still more charge carriers, etc.

  Note that avalanche breakdown is **hysteretic** (that is, after it sets in and the additional charge carriers are created within the depletion layer, the semiconductor continues to conduct even after the voltage is reduced below the breakdown threshold), whereas Zener breakdown is not. Diodes designed to undergo these types of breakdown at specific voltages without being damaged, called **Zener diodes** and **avalanche diodes** respectively, are both useful in electric circuit design.
- **Diffusion** of charge carriers (electrons and holes) across the p-n junction in a diode sets up a small depletion zone and a corresponding **built-in voltage** even when the external voltage applied to the diode is zero. Thus, under forward bias, the applied voltage must exceed a certain **cut-in voltage** V_{d} (0.6 to 0.7 V for silicon diodes, 0.25 to 0.3 V for germanium diodes, and 0.15 to 0.45 volts for Schottky diodes) before current will begin to flow.
- Due to a weak thermodynamic process of **carrier generation and recombination** inside the depletion layer, a small **leakage current** always flows through a diode under reverse bias even when the applied voltage is below the breakdown threshold. Note in particular that
  - **carrier generation** due to the absorption of energy of incident photons, and the resulting current when under forward bias, is how **photodiodes** respond to the intensity of incident light, whereas
  - in **light-emitting diodes** (**LED**s), during **carrier recombination**, energy is released as photons.
- Finally, under both forward bias (with the applied voltage exceeding the cut-in voltage) and reverse bias (with the applied voltage exceeding the breakdown threshold), a diode exhibits a very small amount of electrical **resistance**, thus creating a very steep slope in a plot of I versus V (see Figure 10.13).

Regular diodes are denoted by the symbol  , and both avalanche and Zener diodes by the symbol  , with the arrow pointing in the direction of the current when under forward bias. Real semiconductor diodes are often **axial** (small cylinders with a wire out each end), with the n-doped end marked with a single bar, consistent with the bar at the end of the diode symbol.

10.2.1.2 Bipolar Junction Transistors (BJTs)

A semiconductor crystal designed to behave as an **amplifier** or an **electronically-activated switch** is called a **transistor**, and is built from three adjacent doped regions of alternating type. As depicted in Table 10.7, there are essentially eight main types of transistors, which are all somewhat similar in their application, though they differ considerably in their physical construction and internal operation. A **bipolar junction transistor** (**BJT**) is the most robust and common type of transistor. A BJT is, in effect, two oppositely-facing diodes placed back-to-back in a single semiconductor crystal. As suggested by their respective names and symbols,

- in a p-n-p type BJT, the emitter-base connection is a p-n diode nominally under forward bias, whereas
- in an n-p-n type BJT, the base-emitter connection is a p-n diode nominally under forward bias.

If the middle section of a BJT, called the **base**, is left unconnected, then (in the ideal setting, assuming no breakdown) there will be zero current between the two ends of the BJT (called the **emitter** and the **collector**), as one of its two p-n junctions will always be under reverse bias. If (in the p-n-p case) a small **emitter** $\rightarrow$ **base** current (or, in the n-p-n case, a small **base** $\rightarrow$ **emitter** current) is initiated, this populates the central region of the transistor (including the depletion zone in the p-n junction between the base and the collector, which is nominally under reverse bias) with charge carriers, thus causing a much larger current between the emitter and collector to flow, proportional to the current at the base. We denote the voltages and the magnitude of the currents of the emitter, base, and collector as, respectively, $\{V_{\mathrm{E}}, V_{\mathrm{B}}, V_{\mathrm{C}}\}$ and $\{I_{\mathrm{E}}, I_{\mathrm{B}}, I_{\mathrm{C}}\}$; note that $I_{\mathrm{E}} = I_{\mathrm{C}} + I_{\mathrm{B}}$ in both n-p-n and p-n-p type BJTs. Assuming the voltage differences are sufficiently small that breakdown does not set in, the three useful modes of operation of a **n-p-n transistor** depend on where V_B is with respect to V_C and V_E, with $V_C > V_E$ (the p-n-p case is similar, with all inequalities reversed):

- **Saturation** or "**on**" mode: $V_B > V_C > V_E$. Both p-n junctions are forward biased; current flows freely (small effective resistance $R_{CE(\mathrm{on})}$), limited by resisters elsewhere in the circuit. Energetically efficient!
- **Forward active** or "**linear**" mode: $V_{\mathrm{C}} > V_{\mathrm{B}} > V_{\mathrm{E}}$. This is the nominal setting in which the transistor acts as a current amplifier, as used in many audio systems. The **current gain** from I_{B} to I_{C} in this mode is denoted h_{FE} or β_{F}, and is typically about $h_{\mathrm{FE}} = \beta_{\mathrm{F}} = I_{\mathrm{C}}/I_{\mathrm{B}} \approx 100$, whereas the ratio $I_{\mathrm{C}}/I_{\mathrm{E}}$ is denoted α_{F}, and is typically about $\alpha_{\mathrm{F}} = I_{\mathrm{C}}/I_{\mathrm{E}} = \beta_{\mathrm{F}}/(1+\beta_{\mathrm{F}}) \approx 0.99$. *Not* energetically efficient.
- **Cutoff** mode: $V_C > V_E > V_B$. Both p-n junctions are reverse biased; very little current flows. Efficient!

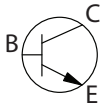
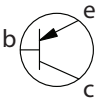
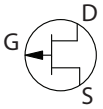
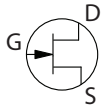
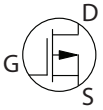
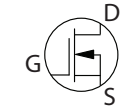
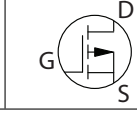
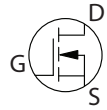
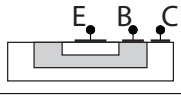
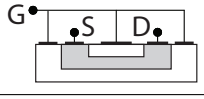
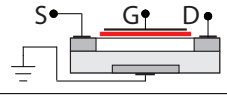
Bipolar Junction Transistor (**BJT**)		Field-Effect Transistor (**FET**)					
		Junction FET (**JFET**) (depletion mode)		Insulated-Gate FET (**IGFET**)			
				depletion mode		enhancement mode	
n-p-n type	p-n-p type	p-channel	n-channel	p-channel	n-channel	p-channel	n-channel
							
							

Table 10.7: The eight main types of transistors, their symbols, and their essential construction features. The three nodes of a BJT are denoted the **base** (B), **emitter** (E), and **collector** (C), whereas the corresponding nodes of an FET are denoted the **gate** (G), **source** (S), and **drain** (D). The most common type of IGFET is the **MOSFET**.

The fourth mode of an n-p-n transistor, **reverse active** or "**backwards**" mode, given by $V_C < V_E$, is the result of installing the transistor backwards. The construction of a BJT (see Table 10.7) is *not* symmetric (notwithstanding introductory explanations of how a BJT functions, that might initially seem to imply the contrary). In particular, the surface area of the p-n junction between the base and the collector needs to be much larger than the surface area of the p-n junction between the base and the emitter for the BJT to perform well. The current gain of a BJT in reverse active mode is typically quite poor; this mode is thus to be avoided.

Noting that I_B is typically much smaller than I_C, the power dissipated by a BJT is nearly $P = |V_C - V_E|\, I_E$ [similarly, the power dissipated by a FET is nearly $P = |V_D - V_S|\, I_S$]. A transistor operating in the linear region is *not* power efficient; in audio applications, these diminutive devices may dissipate many watts of power in linear mode, often necessitating heat sinks. On the other hand, when used as a switch (in both saturation and cutoff modes), very little power is dissipated by a transistor (BJT or FET); further, modern transistors (MOSFETs in particular) can switch from saturation (full on) to cutoff (full off), or back, in *tens of nanoseconds*. Thus:

Guideline 10.1 *For power-efficient operation of transistors, use them as fast switches rather than amplifiers.*

As mentioned above, the **simplest model of a BJT in forward active mode** is as a current amplifier,

$$I_C = \beta_F\, I_B, \quad I_C = \alpha_F\, I_E \quad \text{with} \quad \alpha_F = \beta_F/(1+\beta_F) \tag{10.11a}$$

and the **current gain** β_F (aka h_{FE}) taken as a (large) constant, with $\beta_F \approx 100$ and thus $\alpha_F \approx 0.99$ as typical values. The more accurate **Early model** of forward active mode models β_F as a function of the magnitude of the collector-emitter voltage $V_{CE} = |V_C - V_E|$ such that

$$\beta_F = (1 + V_{CE}/V_A)\, \beta_{F0} \tag{10.11b}$$

in (10.11a), where the constants V_A and β_{F0} are called the **Early voltage** and the **current gain at zero bias**, respectively. This model may be extended to incorporate the base-emitter voltage $V_{BE} = |V_B - V_E|$ such that

$$I_C = (1 + V_{CE}/V_A)\, (e^{V_{BE}/V_T} - 1)\, I_S \quad \Rightarrow \quad I_C \approx I_S\, e^{V_{BE}/V_T} \text{ if } V_{CE}/V_A \ll 1 \text{ and } V_{BE} \gg V_T. \tag{10.11c}$$

where the constants I_S and V_T are referred to as the **reverse saturation current** and the **thermal voltage**, respectively. Typical constant values are $I_S = 10^{-15}$ to 10^{-12} amps, $V_T = 26$ mV, and $V_A = 15$ V to 150 V. Practically speaking, if I_C is non-negligible, $V_{BE} = 0.7$ V is a good approximation for silicon BJTs.

In a manner analogous to BJTs, the main flow of current in a **Field-Effect Transistor** (**FET**), between the **drain** and the **source**, is regulated by the voltage at the **gate** (relative to that at the source). The main distinction between an FET and a BJT is that the drain-source current of a FET is regulated by the *voltage* at the gate, whereas the emitter-collector current of a BJT is regulated by the *current* through the base. FETs come in two main types, Junction FETs and Insulated-Gate FETs.

10.2.1.3 Junction Field Effect Transistors (JFETs)

A **Junction Field-Effect Transistor** (**JFET**) is a (usually, symmetric) transistor design in which the source and drain are connected to the two ends of a single semiconductor channel that is a either n-doped or p-doped. As indicated Table 10.7, adjacent to the channel are oppositely-doped semiconductor regions connected to the gate. A JFET operates in what is known as **depletion mode**: if the gate of the JFET is left disconnected, the (n-doped or p-doped) channel of the JFET readily conducts current from the source to the drain, or from the drain to the source. However, if a voltage is applied to the gate of the appropriate sign such that the p-n junctions along the edge of the channel are reverse-biased, a depletion zone forms in the channel which diminishes the amount of current the JFET channel can conduct between the source and the drain. Increasing the magnitude of the voltage applied to the gate increases the size of this depletion zone, which further diminishes the current that the JFET can conduct between the source and the drain, until a **pinch-off** level is reached, in which the current the JFET can conduct between the source and the drain is essentially reduced to zero.

10.2.1.4 Insulated-Gate Field Effect Transistors (IGFETs, including MOSFETs)

In an **Insulated-Gate Field Effect Transistor** (**IGFET**), the gate is *electrically insulated* from the channel carrying the current between the source and the drain. Again, the semiconductor channel in an IGFET is either n-doped or p-doped. The most common type of IGFET, in which the gate insulation (indicated in red in Table 10.7) is a metal oxide, is known as a **Metal Oxide Semiconductor Field-Effect Transistor** (**MOSFET**). Due to the insulation of the gate, an IGFET has a *very high input impedance*, with almost zero current flowing through the gate. This makes IGFETs particularly efficient in logic circuits or as fast switches; however, the gate insulation of a MOSFET is generally quite susceptible to damage from static electricity. IGFETs come in two classes, those that work in a **depletion mode** similar to that of a JFET as described above, and those that work in an **enhancement mode**, in which the channel (the white region below the red insulation in Table 10.7) between the source and the drain is generally nonconducting (it may even be undoped) until a sufficiently large voltage is applied between the gate and ground, which populates the channel between the source and drain with charge carriers, thus enabling current to flow.

Though the first working transistor was demonstrated way back in 1947, the technology of transistors designed for various different purposes is still evolving rapidly today. In particular, for applications in **digital logic** (CPUs, GPUs, DSPs, etc.), designed for fast power-efficient numerical computation, transistors continue to be shrunk in size, packed more densely together, and reduced in operating voltage (thus improving power efficiency). Such ICs are developed with photolithography fabrication techniques leveraging short wavelength **DUV** (deep ultraviolet, ∼200 nm) and **EUV** (extreme ultraviolet, 13.5 nm) light sources. Using so-called "5 nm" processes, densities of up to 200 MTr/mm^2 (million transistors per mm^2) are now (as of 2021) common in large-scale chip fabrication, with even denser production processes on the foreseeable horizon. Transistor counts in modern high-end microprocessors and GPUs (graphics processing units) are in the tens of billions. In contrast, microcontrollers (MCUs) incorporate *much* more streamlined CPUs (for example, an ARM Cortex M0 has about 12k gates, and thus about 72k transistors); the majority of the transistors on an MCU are associated with cache and memory (as a datapoint, a 64 KiB cache has about 3.1M transistors).

For applications in **power electronics**, transistor technology is also still evolving quickly. Four transistor metrics of interest in high-power applications are particularly important:

• The **effective resistance** of a MOSFET when operating in the "on" state, aka $R_{DS(on)}$. In addition to wasting less power (and thus being able to run on a given battery charge for a bit longer), even more significant in many power protection (reverse-voltage, over-voltage, etc) applications is that reduced values of $R_{DS(on)}$ on the power MOSFET imply much less waste heat generated under normal operating conditions that must be dissipated (on the PCB, and/or with a heat sink), thereby facilitating a higher density integration of power components on the PCB. MOSFETs with values of $R_{DS(on)}$ in the neighborhood of 1 mΩ (‼) are now common.
• The **time delay** from the on state to the off state of the transistor when the gate is triggered, aka $t_{d(off)}$. This measure characterizes how quickly a power protection MOSFET can turn the power off to a system when a fault condition occurs. MOSFETs with values of $t_{d(off)}$ in the neighborhood of 20 to 40 ns (‼) are now common.
• The **rise time** t_r and **fall time** t_f associated with repeated fast switching of the transistor between the on and off states. Many MOSFETs are commonly used for switching power to a device (e.g., an LED) on and off thousands of times a second, an approach referred to as **pulse width modulation** (**PWM**). Averaged over several cycles (e.g., by the human eye), this makes the device look as if it is running at partial power (proportional to the fraction of time that the transistor is in the on state, referred to as the **duty cycle** of the PWM signal). PWM-based driving strategies will be used in multiple circuits discussed in the remainder of this chapter. As discussed previously (see Guideline 10.1), a transistor is generally quite efficient in both the on state and the off state; the time spent switching between these two states is where most of the inefficiencies lie. Thus, at a given switching frequency, the faster the switching time, the more efficient this PWM approach is. MOSFETs with values of t_r and t_f in the neighborhood of 10 to 20 ns (‼) are now common.

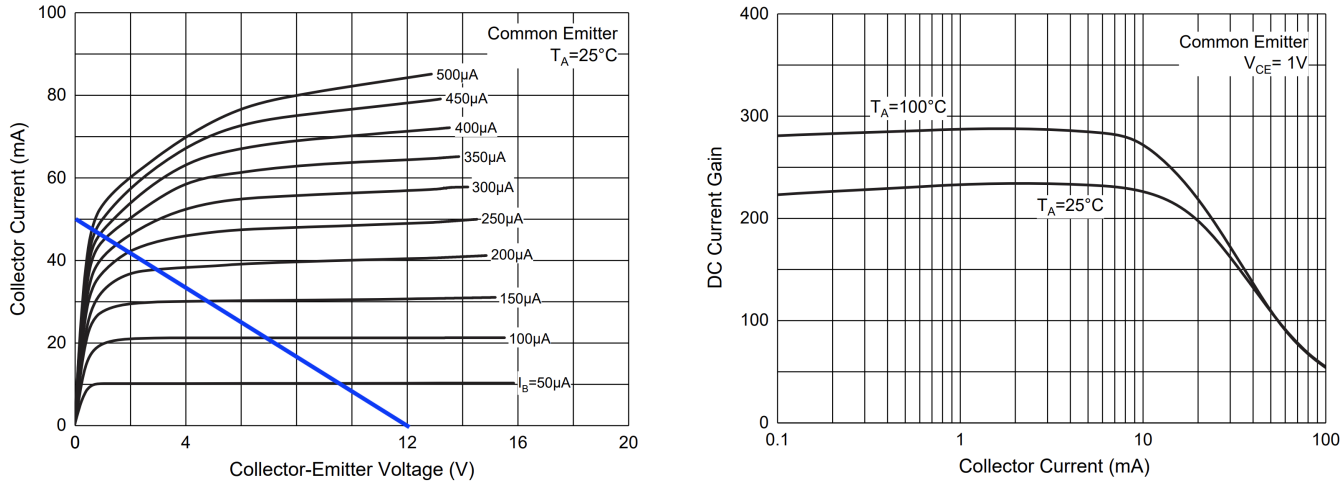


Figure 10.14: Static characteristics of a "typical" general-purpose NPN BJT, the MCC 2N3904. (left) Collector current I_C vs. collector-emitter voltage $V_{CE} = V_C - V_E$ as a function of the base current I_B. (right) DC current gain h_{FE} vs. collector current I_C as a function of the device temperature T_A. The diagonal **load line** connects the $V_{CE,\text{max}}$ point (with $I_C = 0$) to the $I_{C,\text{max}}$ point (with $V_{CE} = 0$), as set up by the supply voltage provided to the circuit, as well as the passive components surrounding the transistor; further explanation of the importance of this line is given on the following page, and Example 10.12.

Examples of modern high-performance MOSFETs include the TI CSD18510Q5B and the CSD88584Q5DC, as used for power protection and BLDC motor control, respectively, in the Beret family of boards (see §5).

10.2.1.5 Static characteristics of BJTs: check the datasheets!

To understand accurately the specific characteristics of interest of any transistor (BJT or FET), it is imperative that you actually examine its datasheet (or, you experimentally measure these characteristics yourself), as there is substantial variation between different transistor designs in the dependence of such characteristics on a range of parameters. BJTs are commonly benchmarked in one of three basic configurations:

- **common base**, with the emitter driven as the (low-imedance) input, and the collector used as the ouput,
- **common collector**, with the base driven as the (high-imedance) input, and the emitter used as the ouput, or
- **common emitter**, with the base driven as the (high-imedance) input, and the collector used as the ouput.

Among these three, the common emitter configuration is considered most often, as it provides both substantial voltage gain and substantial current gain, and thus provides the best overall power gain.

Though many very good online introductions model and/or plot the "typical" behavior of various types transistors (BJTs or FETs) in one or more of these three basic configurations, these characteristics actually vary substantially from one transistor design to the next; again, there is no substitute for examining the datasheet of the device actually to be used.

Notwithstanding the admonitions of the previous two paragraphs, some "representative" characteristics of a "typical" general-purpose NPN BJT are illustrated in Figure 10.14. Note that the variation of I_C with V_{CE} and I_B does *not* accurately follow (10.11a)-(10.11b) over the range of V_{CE} and I_B illustrated, and that the variation of h_{FE} (aka β_F) with both I_C and T_A is significant [representing β_F as a constant, or as simple linear function of V_{CE} only, is a rough approximation at best]. Though various efforts to more accurately model such characteristics are included in circuit simulation tools like PSpice, again, there is no substitute for carefully examining and leveraging the information in the datasheet of the transistor device actually to be used.

Further, as shown in Figure 10.15, modern robust plug-in (3-pin) replacements for single transistors, with quite similar nominal performance characteristics, incorporate complex internal circuitry that robustly protect

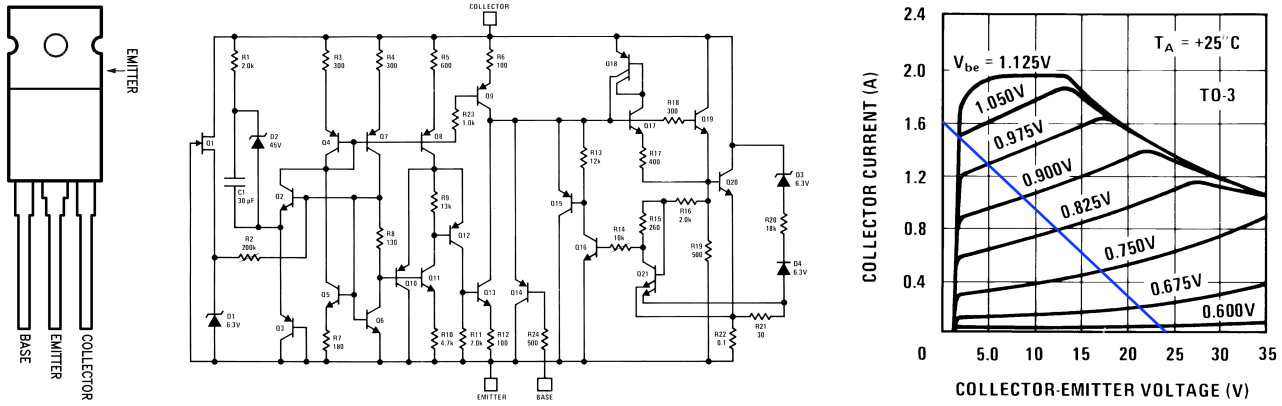


Figure 10.15: A high-reliability replacement for a single NPN BJT, the TI LM395. (left) standard 3-pin package, as used by many BJTs. (center) Complex internal wiring, incorporating various forms of protection circuitry. (right) Collector current I_C vs. collector-emitter voltage V_{CE} as a function of the base-emitter current V_{BE}.

the transistor in the event of a host of possible overload conditions, including the exceeding of safe thermal, current, and power (current times voltage) specifications. Such conditions would otherwise most certainly cause a simple single transistor to fail. Due to their similar performance to simple BJTs in the vicinity of the load line (where the transistor is normally operated, see next subsection), they may be used as simple plug-in replacements for single transistors in many circuits.

10.2.1.6 Load line

Fortunately, when implementing transistors properly into amplifier circuits that leverage them, as discussed in the many examples provided below (see in particular Example 10.12), the gain of the overall amplifier is governed primarily by the passives surrounding the transistor, and *not* by the specific I_B -to- I_C or V_{BE} -to- I_C gain characteristics of the transistor itself (recall that these characteristics vary significantly from one transistor to another, and depend strongly on operating temperature, the current at the collector, etc.), as long as this gain is sufficiently large.

The design process for transistor-based amplifiers generally involves drawing a diagonal **load line** (see, e.g., Figures 10.14a and 10.15c) from two extreme operating conditions:

- the maximum possible voltage V_{CE} across the transistor (usually, the supply voltage) when $I_C = 0$, and
- the maximum possible current I_C through the transistor when it is "saturated" (that is, when $V_{CE} = 0$).

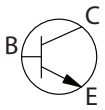
[Again, these conditions are generally defined by the circuit around the transistor, not by the transistor itself.] The voltage biasing that sets up the nominal conditions at the gate (as illustrated in Figure 10.3c, and discussed further in Example 10.12) is then arranged to operate nominally near the center (referred to as the "Q point") of the "linear part" of this range in the V_{CE} to I_C relationship, with variations in the input (I_B or V_{BE}) around this Q point creating an approximately linear response in the output I_C.

The region to the extreme left in the collector current I_C vs. collector-emitter voltage V_{CE} plot (see Figures 10.14a and 10.15c, and note where the several curves depicting the various possible conditions at the gate collapse into a single steep line) is sometimes called the **saturation region** or **ohmic region**. In this region, the middle of the transistor is effectively "saturated" with charge carriers, and the transistor "acts" effectively like a resistor, with a relatively small resistance (that is, $V_{CE} = I_C R_{CE(\text{on})}$), independent of the precise conditions at the base.

To the right of the saturation region is the **forward active region**, where (in the n-p-n case) $V_C > V_B > V_E$, and below that is the **cutoff region**, where (approximately) $V_C > V_E > V_B$, as discussed further on page 10-21.

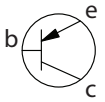
As described on page 10-21, the three useful modes of operation of an **n-p-n** BJT (with $V_C > V_E$) are:

- **saturation** (with V_B above both V_C and V_E),
- **linear** (with V_B between V_C and V_E), and
- **cutoff** (with V_B below both V_C and V_E),

n-p-n BJT: 

and the three useful modes of operation of a **p-n-p** BJT (with $V_e > V_c$, switching to lowercase e, b, c for notational clarity), are:

- **cutoff** (with V_b above both V_e and V_c),
- **linear** (with V_b between V_e and V_c), and
- **saturation** (with V_b below both V_e and V_c).

p-n-p BJT: 

There are many ways to build an **amplifier** with such transistors for various applications, including
- the amplification of audio signals (for playing sounds on speakers, including woofers, tweeters, and mids),
- the amplification of the very-low-amplitude signals from analog sensors, like piezos and thermocouples,
- the (AM or FM) transmission of radio frequency (RF) signals, etc.

Amplification systems may also be built by *cascading* multiple amplifier stages (e.g., a **pre-amplifier** followed by a **power amplifier**). Individual amplifier stages are classified by the number of degrees that their transistors are held in linear mode (i.e., the so-called **conduction angle**) during the amplification of a sinusoidal input:

Class A amplifiers include a single transistor that is held in linear mode for 360 degrees (100% of the time).
Class B amplifiers include two transistors, each held in linear mode for almost 180 degrees (50% of the time)[19].
Class AB amplifiers include two transistors, each held in linear mode for somewhat *more* than 180 degrees[20].
Class C amplifiers include two transistors, each held in linear mode for significantly *less* than 180 degrees[21].
Class D amplifiers are built for the amplification of binary or ternary PWM signals[22].

Other amplifier classes primarily represent various improvements to the fundamental classes listed above. Though a complete presentation of this fascinating subject is beyond the scope of this discussion, a brief introduction to representative designs in a few of the above classes is in order.

Example 10.12 A representative **Class A amplifier**, built around a single n-p-n BJT, is given in Figure 10.16a. Denoting $\{V_C, V_B, V_E\}$ and $\{I_C, I_B, I_E\}$ as the voltage and current at the collector, base, and emitter of the BJT (positive current to the right and down), noting $I_4 = I_E$, and assuming[23] that the BJT is operating in linear mode 100% of the time under normal operation, the equations governing the BJT in this design are

$$I_{\rm E} = I_{\rm B} + I_{\rm C}, \quad I_{\rm C} = \alpha_{\rm F}\, I_{\rm E}, \quad V_{\rm B} - V_{\rm E} \approx V_d\,; \tag{10.12a}$$

the rest of the component and KCL equations governing this circuit are determined as in previous examples[24]:

$$I_0 = C_0\, d(V_{\rm in} - V_B)/dt, \quad V_s - V_B = I_1 R_1, \quad V_B = I_2 R_2, \quad I_0 + I_1 = I_2 + I_B, \tag{10.12b}$$

$$I_3 = I_{\rm C} + I_5, \quad V_s - V_{\rm C} = I_3 R_3, \quad V_E = I_E R_4, \quad I_5 = C_5\, d(V_C - V_{\rm out})/dt, \quad V_{\rm out} = I_5\, R_{\rm speaker}. \tag{10.12c}$$

[19] The Class B approach approximately doubles the power efficiency of the Class A approach, but often exhibits significant **crossover distortion** during the time in which one transistor is shifting out of cutoff mode, and the other is shifting into cutoff mode, as these processes happen somewhat gradually as the input signal changes.

[20] The slight overlap of the "on" time of each of the two transistors when amplifying a sinusoidal signal in the Class AB approach is helpful in reducing the crossover distortion exhibited by a pure Class B approach.

[21] A Class C amplifier is often used to excite an LC oscillator that may be tuned to resonate at a particular frequency (e.g., for the modulation of an RF transmission). The LC oscillator establishes the underlying sinusoidal nature of the output; a Class C amplifier on its own (not exciting such an oscillator) would otherwise introduce significant distortion to an incoming signal.

[22] Leveraging modern fast-switching MOSFETs, the Class D approach, feeding into a second-order low-pass LC filter that efficiently averages the output (removing the oscillations at the underlying PWM frequency) can achieve very high (over 90%) efficiency.

[23] Once our analysis of the circuit is established, we will tune the passives in the circuit to assure this assumption is satisfied.

[24] We (roughly) model the speaker here as a purely resistive load with resistance $R_{\rm speaker}$; see Example 10.9 for further discussion.

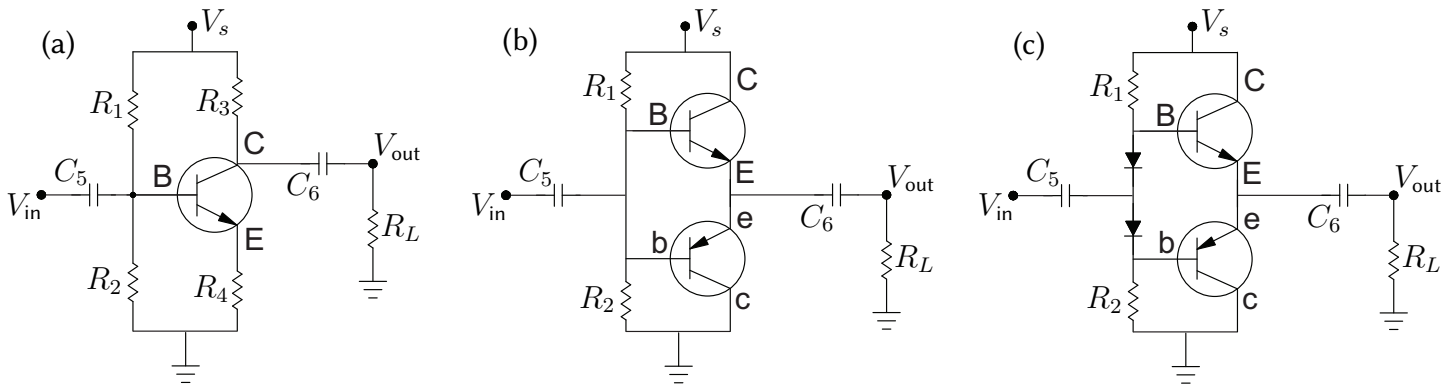


Figure 10.16: Typical embodiments of three different classes of simple BJT-based amplifiers:
(a) Class A, with a single n-p-n transistor with a $360°$ conduction angle.
(b) Class B ("push-pull"), with a matched pair of n-p-n and p-n-p transistors, each with $180°$ conduction angle.
(c) Class AB, with a matched pair of transistors each with conduction angle somewhat greater than $180°$.

Our full system has 12 eqns in the 12 variables $\{V_{\text{out}}, V_C, V_B, V_E, I_C, I_B, I_E, I_0, I_1, I_2, I_3, I_5\}$, plus the input signal V_{in}, the source voltage V_s, the transistor constants $\{\alpha_{\text{F}}, V_d\}$, and the passives $\{C_0, R_1, R_2, R_3, R_4, R_{\text{speaker}}\}$. These 12 linear equations are easily Laplace transformed and combined.

For large β_F [and thus $\alpha_F \approx 1$] and appropriate choices for $\{R_1, R_2\}$, $I_B(t)$ is negligible in (10.12b), and the transfer function governing how $V_{\text{out}}(s)$ responds to $V_{in}(s)$ essentially decouples into two cascaded parts: (i) one from $V_{in}(s)$ to $V_B(s)$ via $\{C_0, R_1, R_2\}$, (ii) one from $V_B(s)$ to $V_{\text{out}}(s)$ via the transistor and $\{R_3, R_4, C_5\}$ [in the present analysis, V_{out} is also routed through a speaker, with characteristic resistance R_{speaker}, to ground]. This decoupling provides particular insight; we thus derive these two separate transfer functions here.

For part (i) in this large β_F limit, it is seen that $\{C_0, R_1, R_2\}$ amount simply to a **biased first-order high-pass filter with unit gain**, exactly as in Figure 10.3c; this is seen by combining the 4 eqns in (10.12b) together with $I_B \approx 0$, in the 5 variables $\{I_0, I_1, I_2, I_B, V_B\}$, and the input V_{in}, which immediately gives

$$V_{\text{B}}(s) = \frac{R_2\, V_s}{R_1 + R_2 + R_1\, R_2\, C_0\, s} + \frac{R_1\, R_2\, C_0\, s\, V_{\text{in}}(s)}{R_1 + R_2 + R_1\, R_2\, C_0\, s} = \frac{R_2}{R_1 + R_2}\, \frac{\omega_{\text{i}}}{s + \omega_{\text{i}}}\, V_s + \frac{s}{s + \omega_{\text{i}}}\, V_{\text{in}}(s),$$

where $R_i = R_1 R_2/(R_1 + R_2)$ [that is, $1/R_i = 1/R_1 + 1/R_2$] and the cutoff frequency is $\omega_{\text{i}} = 1/(R_i\, C_0)$. The voltage divider biasing drives the steady component of $V_B(t)$ towards $V_Q = V_s\, R_2/(R_1 + R_2)$ [instead of towards zero, as done by the filter in Figure 10.3b, which effectively takes $R_1 \to \infty$ in Figure 10.3c].

For part (ii) in the large β_F limit, it is found that the transistor (assumed to be operating in the linear mode) and $\{R_3, R_4, C_5\}$ amount simply to another first-order high-pass filter with negative gain; this is seen by combining the 8 eqns in (10.12a) and (10.12c), in the 8 variables $\{I_C, I_B, I_E, V_C, V_E, I_3, I_5, V_{\text{out}}\}$, together with the input $V_B(t)$, which immediately (see RR_Amplifier_Class_A.m) gives:

$$V_{\text{out}}(s) = \frac{C_5\, R_{\text{speaker}}\, s}{(R_3 + R_{\text{speaker}})\, C_5\, s + 1}\, V_s - \alpha_F\, \frac{R_3}{R_4}\, \frac{R_{\text{speaker}}\, C_5\, s}{(R_3 + R_{\text{speaker}})\, C_5\, s + 1}\, (V_B - V_d) = V_{\text{ii}}(s) + K\, \frac{s}{s + \omega_{\text{ii}}}\, V_B(s)$$

where $K = -\alpha_{\text{F}}\, (R_3/R_4)\, [R_{\text{speaker}}/(R_3 + R_{\text{speaker}})]$, the cutoff frequency of the high-pass filter on $V_B(t)$ is $\omega_{\text{ii}} = 1/(R_{ii}\, C_0)$ where $R_{ii} = R_3 + R_{\text{speaker}}$, and the component $V_{\text{ii}}(s)$ is driven solely by the voltages V_s and V_d, and quickly approaches a constant. For finite values of R_{speaker}, by Fact 9.4, $V_{\text{ii}}(t)$ goes to zero as $t \to \infty$, as the connection of V_{out} to ground (through the speaker) charges C_5. As $I_5(t) = V_{\text{out}}(t)/R_{\text{speaker}}$, it follows that $I_5(t) \to 0$ as $t \to \infty$. In the case that $R_3 \ll R_{\text{speaker}}$ (e.g., if the speaker is removed), $K \approx -\alpha_{\text{F}}\, (R_3/R_4)$.

When the input signal is time varying, the following two extreme cases are of interest:

• when V_B is near its maximum, V_s, the transistor is nearly saturated, $V_{CE} \approx 0$, and thus $I_{C,\text{max}} \approx V_s/(R_3+R_4)$;
• when V_B is near its minimum, 0, the transistor is nearly in cutoff, and $I_{C,\text{max}} \approx 0$.

When the input signal is constant (i.e., $V_B \approx V_s/2$, the transistor is near the center of its linear active region ($V_{CE} \approx V_s/2$; see discussion of the load line in §10.2.1.6), and substantial current flows, $I_{C,\text{quiescent}} \approx I_{C,\text{max}}/2$. As a result, Class A amplifier designs, though accurately linear in behavior, are generally also quite inefficient.

Consider now an application with $V_d = 0.7\,V$ (the cut-in voltage for a silicon BJT), a typical n-p-n BJT with $\beta_F \approx 100 \Rightarrow \alpha_F \approx 0.99$, a speaker with $R_{\text{speaker}} = 8\,\text{ohm}$, and a supply voltage of $V_s = 12\,\text{V}$:

• For part ii, design targets of $I_{C,\text{max}} = 50\,\text{mA}$ (see Figure 10.14) and thus $R_3 + R_4 = V_s/I_{C,\text{max}} \approx 240$ ohm, $\omega_{ii} = 1/(R_{ii}\,C_5) \approx 10$ Hz, and $K \approx 10$ lead to values of $\{R_3, R_4, C_5\} \approx \{239.2\,\text{ohm}, 0.8\,\text{ohm}, 400\,\mu\text{F}\}$. In the case that $R_{\text{speaker}} \to \infty$, these design targets give $\{R_3, R_4\} \approx \{218.4\,\text{ohm}, 21.6\,\text{ohm}\}$, and C_5 can be removed.

• For part i, we desire V_Q (i.e., the steady component of V_B) to be about $V_s/2$, and $I_{B,\text{max}} \approx I_{C,\text{max}}/\beta = 0.5\,\text{mA}$ to be relatively small in $I_0 + I_1 = I_2 + I_B$. This may be achieved by taking $I_1 \approx I_2 \approx 10\,\text{mA}$, and thus $R_1 + R_2 = 12/0.010 = 1.2\,\text{kohm}$, or $R_1 = R_2 \approx 600\,\text{ohm}$. The design target $\omega_i = 1/(R_i\,C_0) \approx 10$ Hz then gives $C_0 \approx 330\,\mu\text{F}$ (see RR_Amplifier_Class_A.m for calculations). △

Example 10.13 A representative **Class B amplifier**, built around a matched pair of n-p-n and p-n-p BJTs, is given in Figure 10.16b. The $\{C_5, R_1, R_2\}$ components, with $R_1 = R_2$, again provide high-pass filtering with voltage divider biasing at the input stage, the output of which is applied to the base of both the (upper) n-p-n BJT and the (lower) p-n-p BJT. Note also that the emitters of both BJTs are tied together, and that the C_6 component into R_L at the output stage again provides high-pass filtering which eliminates the DC ouput current.

With this simple "push-pull" configuration, the base voltage $V_B = V_b$ is either:

(a) above $V_E = V_e$, in which case the n-p-n BJT is in linear active mode and the p-n-p BJT is in cutoff, or
(b) below $V_E = V_e$, in which case the p-n-p BJT is in linear active mode and the n-p-n BJT is in cutoff.

Thus, in this basic Class B design, either one of these BJTs is "on", and amplifying the input in accordance with the model $I_C \approx I_S\, e^{V_{BE}/V_T}$ [see (10.11c)], or the other BJT is on; they are never both "on" simultaneously.

Looking a bit more closely [see, in particular, Figure 10.13], it actually takes the V_{BE} junction to be slightly *above* a small cut-in voltage V_d (in silicon, $V_d \approx 0.7\,\text{V}$) before the n-p-n BJT enters linear active mode, and it takes the V_{eb} junction to be slightly *below* $-V_d$ before the p-n-p BJT enters linear active mode. As a result, there is a range of (small) inputs V_{in}, referred to as a "dead zone", for which both BJTs remain in cutoff, and the output current is zero. The resulting lack of linearity in the response, which is especially pronounced for small input signals, is referred to as **crossover distortion**. As both BJTs are actually in cutoff for zero (or, small) inputs, however, Class B amplifier designs are generally much more efficient than Class A amplifier designs.

Despite the crossover distortion mentioned above, this simple "push-pull" configuration is useful in applications in which a linear response is not especially important; a typical example[25] is the output stage of a power op amp, such as the TI ALM2402-Q1 included in the Berets, as discussed in §5. △

Example 10.14 A **Class AB amplifier**, as illustrated in Figure 10.16c, is a tweak on the Class B amplifier design which adjusts the bias V_B to be about $2\,V_d \approx 1.4\,\text{V}$ above V_b. This has the effect of effectively eliminating the dead zone of the Class B amplifier mentioned previously. As the transition between cutoff and active mode of the transistors is actually somewhat gradual, diodes are usually selected, carefully, with slightly larger V_d than base-emitter junctions of the two transistors, thus slightly overlapping the regions in which the two diodes are on (that is, increasing their conduction angles to somewhat more than 180 degrees), in an effort to minimize crossover distortion, at the cost of a slight reduction in efficiency. △

[25] Note that op amps (see §10.3) are characterized by very high gain, and are invariably used in *feedback* configurations, and thus their precise gain characteristics are actually rather unimportant.

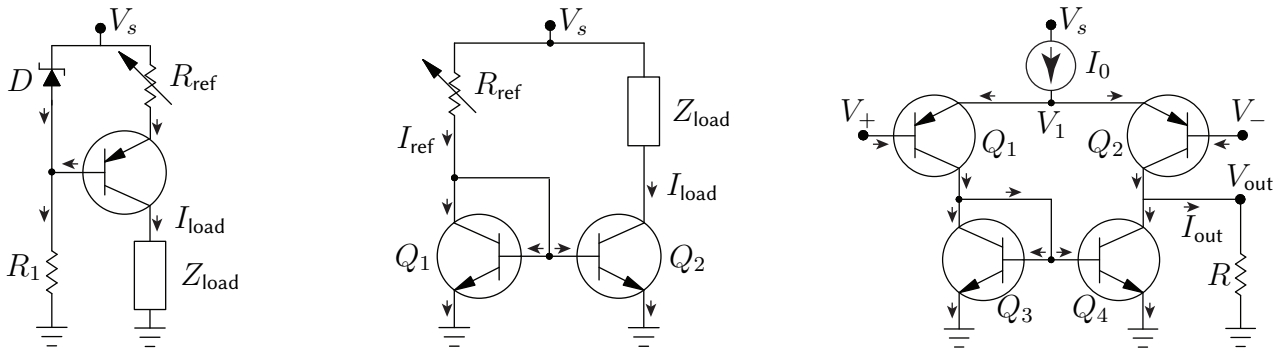


Figure 10.17: Simple transistor circuits. (a) A **current source** based on a p-n-p BJT and a Zener diode, with $I_{\text{load}} \approx (V_{\text{br}} - V_{\text{eb}})/R_{\text{ref}}$. (b) A **current mirror** based on two n-p-n BJTs, with $I_{\text{load}} \approx I_{\text{ref}} = (V_s - V_{\text{BE}})/R_{\text{ref}}$. (c) A **differential amplifier** based on four BJTs and a current source, as in (a), with $V_{\text{out}} \approx D(V_+ - V_-)$ where $D = I_{\text{S}}\, R/V_{\text{T}}$; note that the lower half of this circuit is exactly the current mirror considered in (b).

Other amplifier designs, including minor variations of these typical embodiments, are easily found online. We now present a handful of other useful transistor-based circuit designs.

Example 10.15 Current source. Consider first the circuit in Figure 10.17a. As discussed previously (see Figure 10.13), a Zener diode under a sufficiently large reverse bias has an essentially constant voltage drop across it, V_{br}, regardless of the current flowing through it; note that the resistor R_1 in this circuit limits this Zener diode current. The Zener breakdown voltage V_{br} is also applied across the series connection of the resistor R_{ref} and the emitter-base terminals of the transistor in this circuit; the voltage across resister R_{ref} is thus given by $V_{\text{br}} - V_{\text{eb}}$, where V_{eb} is the voltage drop between the emitter and base of the transistor (about 0.7V for silicon). The emitter current of the transistor is thus given by $I_{\text{e}} = (V_{\text{br}} - V_{\text{eb}})/R_{\text{ref}}$; since V_{br} and V_{eb} are approximately constant, I_{e} is approximately constant. Finally, since a BJT acts as a current amplifier with $I_{\text{b}} = \beta_{\text{F}}\, I_{\text{c}}$ where $\beta_{\text{F}} \approx 100$, it follows that $I_{\text{e}} \approx I_{\text{c}} = I_{\text{load}}$ regardless of the precise values of V_s and β_{F}, provided they are sufficiently large, and regardless of the precise values of R_1 and $|Z_{\text{load}}|$, provided they are sufficiently small. △

Example 10.16 Current mirror. Consider the circuit in Figure 10.17b. Assuming $V_{\text{CE}} \ll V_{\text{A}}$ and thus $\beta_{\text{F}} \approx \beta_{\text{F0}}$ in (10.11b), which is often a good assumption, it follows from (10.11c) that I_{C} of transistor Q_1 is related (exponentially) to V_{BE} such that $I_{\text{C}} = I_{\text{S}}\, e^{V_{\text{BE}}/V_{\text{T}}}$. Since the base-emitter voltage of the (matched) transistors Q_1 and Q_2 are precisely equal in this circuit, their collector currents are equal as well. Finally, since the base currents are negligible compared with the collector currents, it follows from KCL that $I_{\text{load}} \approx I_{\text{ref}}$. △

Example 10.17 Differential amplifier. Consider the circuit in Figure 10.17c. Let $\{V_{\text{E}_k}, V_{\text{B}_k}, V_{\text{C}_k}\}$ and $\{I_{\text{E}_k}, I_{\text{B}_k}, I_{\text{C}_k}\}$ denote the voltage and current of the emitter, base, and collector, respectively, of transistor Q_k, with positive current in the directions indicated in the figure. Due to the current mirror in the lower half of the circuit (see Example 10.16 and Figure 10.17b), $I_{\text{C}_1} \approx I_{\text{C}_4}$. Taking $V_{\text{CE}}/V_{\text{A}} \ll 1$ in (10.11c), and assuming that both $(V_1 - V_+)/V_{\text{T}} \ll 1$ and $(V_1 - V_-)/V_{\text{T}} \ll 1$, noting that $e^{\epsilon} \approx 1 + \epsilon$ for $\epsilon \ll 1$, it follows that

$$\left.\begin{aligned} I_{\text{c}_1} &= I_{\text{S}}\,(e^{(V_1 - V_+)/V_{\text{T}}} - 1) = \alpha_{\text{F}}\, I_{\text{e}_1} \\ I_{\text{c}_2} &= I_{\text{S}}\,(e^{(V_1 - V_-)/V_{\text{T}}} - 1) = \alpha_{\text{F}}\, I_{\text{e}_2} \\ I_0 &= I_{\text{e}_2} + I_{\text{e}_1} \\ I_{\text{out}} &= I_{\text{c}_2} - I_{\text{C}_4} \approx I_{\text{c}_2} - I_{\text{c}_1} \end{aligned}\right\} \Rightarrow \begin{aligned} I_0 &\approx \frac{I_{\text{S}}}{\alpha_{\text{F}}}\Big(\frac{V_1 - V_-}{V_{\text{T}}} + \frac{V_1 - V_+}{V_{\text{T}}}\Big) \;\Rightarrow\; V_1 \approx \frac{1}{2}\Big[\frac{V_{\text{T}}\,\alpha_{\text{F}}\, I_0}{I_{\text{S}}} + V_+ + V_-\Big], \\ I_{\text{out}} &\approx I_{\text{S}}\Big(\frac{V_1 - V_-}{V_{\text{T}}} - \frac{V_1 - V_+}{V_{\text{T}}}\Big) = \frac{I_{\text{S}}}{V_{\text{T}}}\Big(V_+ - V_-\Big), \\ V_{\text{out}} &= I_{\text{out}}\, R \approx D(V_+ - V_-) \quad \text{with} \quad D = I_{\text{S}}\, R/V_{\text{T}}. \end{aligned}$$

Taking V_+ and V_- as the inputs, note that V_{out} responds primarily to the **differential voltage** $(V_+ - V_-)$, while $V_1 = V_{\text{e}_1} = V_{\text{e}_2}$ "floats" up and down in response to the **common voltage** $(V_+ + V_-)$. △

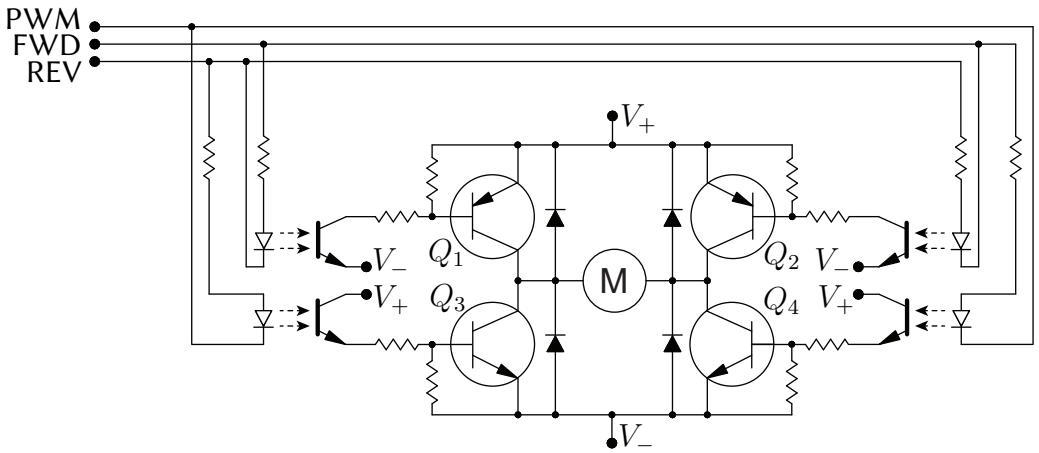


Figure 10.18: Representative H-bridge circuit for efficient bidirectional operation of a BDC motor at partial power via a PWM signal and two GPIOs. All three of these MCU output signals are electrically isolated from the power electronics via **optoisolators**, which are simply LEDs packaged in close proximity with photodiodes.

Example 10.18 H-bridges for driving Brushed DC motors. Brushed DC (BDC) motors are remarkably inexpensive and efficient for converting electrical power to mechanical (rotatary) power. They do not, however, operate effectively at low voltage, due to stiction (that is, dry friction) acting within the motor (see, e.g., the BDC motor model developed in §6.8), thus motivating a PWM-based control approach. They also have significant inductance, as they contain coils of wires, wrapped around ferromagnetic cores, acting as electromagnets; PWM approaches must therefore be implemented with significant caution.

A representative **H-bridge** implementing a PWM-based solution for driving BDC motors at partial power, in a bidirectional fashion, is shown in Figure 10.18. Such H-bridges implement **flyback diodes** to ensure that the voltages at the motor terminals effectively remain between $V_- - V_{\text{br}}$ and $V_+ + V_{\text{br}}$, thus preventing the generation of sparks even when driving motors with substantial inductance. The H-bridge circuit shown in Figure 10.18 operates in four distinct modes, as illustrated in Figure 10.19, based on the FWD and REV logic states:

- **Forward drive/brake** (FWD = 1, REV = 0). In this mode, Q_1 is on, Q_4 is on the same percentage of time that the PWM signal is low, and Q_2 and Q_3 are off. DC power is thus provided from left to right across the motor at a duty cycle set by the PWM. When the PWM signal is high, Q_4 is off, and the current recirculates in the top loop of the bridge through the flyback diode next to Q_2, and the motor "brakes" (see below).
- **Reverse drive/brake** (FWD = 0, REV = 1). In this mode, Q_2 is on, Q_3 is on the same percentage of time that the PWM signal is low, and Q_1 and Q_4 are off. DC power is thus provided from right to left across the motor at a duty cycle set by the PWM. When the PWM signal is high, Q_3 is off, and the current recirculates in the top loop of the bridge through the flyback diode next to Q_1, and again the motor "brakes".
- **Brake/coast** (FWD = 1, REV = 1). In this mode, Q_3 and Q_4 are on the same percentage of time that the PWM signal is low, and Q_1 and Q_2 are off. The braking mode essentially shorts together the two terminals of the motor at a duty cycle set by the PWM; this braking action effectively negates the back emf otherwise generated by the free rotation of the motor, thus causing the motor to slow down. When the PWM signal is high, all four transistors are off, and the motor "coasts" (see below).
- **Coast** (FWD = 0, REV = 0). In this mode, Q_1, Q_2, Q_3 and Q_4 are all off, regardless of the PWM signal. No extra torque is generated by the motor. If the motor momentum and load are such that a significant current is generated in one direction through the motor or the other, this current is sustained by pulling current up from V_- through a flyback diode on one side of the bridge, and pushing this current up through a flyback diode to V_+ on the other side of the bridge, thereby converting mechanical power to electrical power, storing energy back in the battery. Coast mode can thus also be considered as **regenerative braking**.

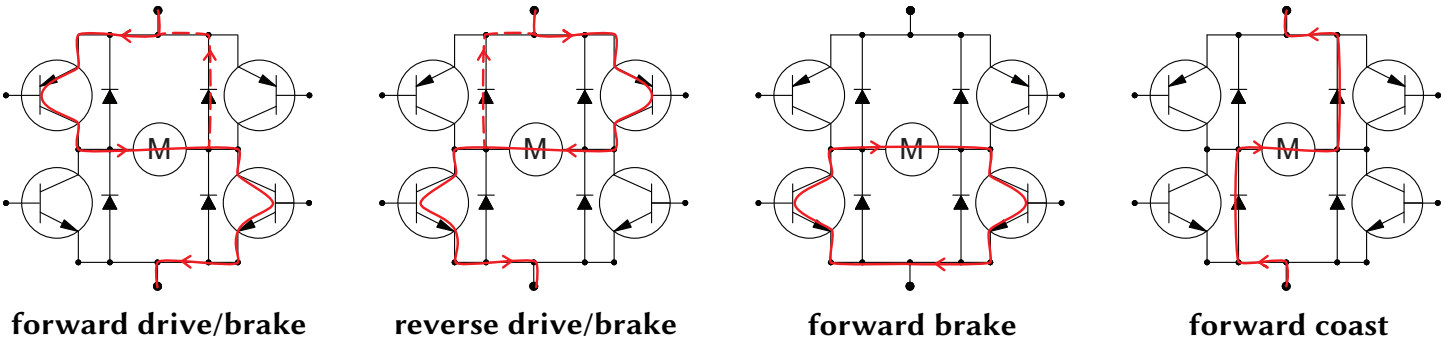


Figure 10.19: Current flow in the four modes of the H-bridge circuit illustrated in Figure 10.18. Note that the use of **high-speed** flyback diodes, which turn on quickly when put under forward bias, are essential in order to keep the voltage at the motor terminals in a limited range, thus preventing the buildup of large voltages and the generation of sparks during the PWM cycle when operating, particularly for motors with large inductance.

In practice, the use of ICs implementing an entire H-bridge circuit are often convenient, such as the Toshiba TB6612FNG, which implements the H-bridge illustrated in Figure 10.18, using MOSFETs instead of BJTs to increase efficiency.

The condition that must absolutely be avoided at all times is both transistors on the same side of an H-bridge being open at the same time, which leads to a short circuit between power and ground. The circuit of Figure 10.18 inherently prevents such a short condition from happening. Other more flexible circuit designs, with more independent control of the four transistors in the bridge, require the appropriate controller logic to be implemented to prevent a short condition. Dedicated motor driver ICs reliably implement such logic.

One feature that other H-bridge circuits (and the motor driver ICs that implement them) can facilitate is the implementation of **drive/coast** modes as an alternative to **drive/brake** modes; that is, the use of "coast" (aka "regenerative braking") during the "off" phase of the PWM when driving, which is energetically more efficient than drive/brake. Some of the more flexible dedicated motor driver ICs, like the remarkable TI DRV8912-Q1 motor drivers implemented by the Berets (see §5.3), internally generate their own PWMs, and allow the user to select between the drive/brake and the drive/coast modes of operation.

Note finally that, as BDC motors sometimes draw very substantial current, the voltage drop across the flyback diodes can be associated with significant power loss and heat generation. Advanced motor driver ICs, like the one mentioned in the previous paragraph, thus turn on the corresponding transistor (which has a much lower effective resistance, aka $R_{\text{DS(on)}}$, than a regular diode) whenever it is detected that current would otherwise flow through a flyback diode, thereby substantially reducing the associated power loss and corresponding heat generation in the device. △

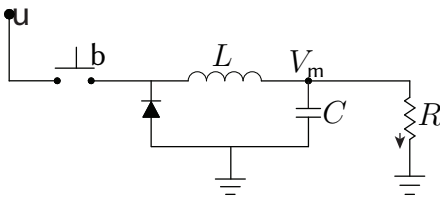


Figure 10.20: Essential components of a buck converter.

Example 10.19 Buck converters. Buck converters are used for DC-to-DC voltage conversion, to step from one voltage (e.g., from a battery) down to a well-regulated lower voltage. The essential components of a buck converter are illustrated in Figure 10.20. △

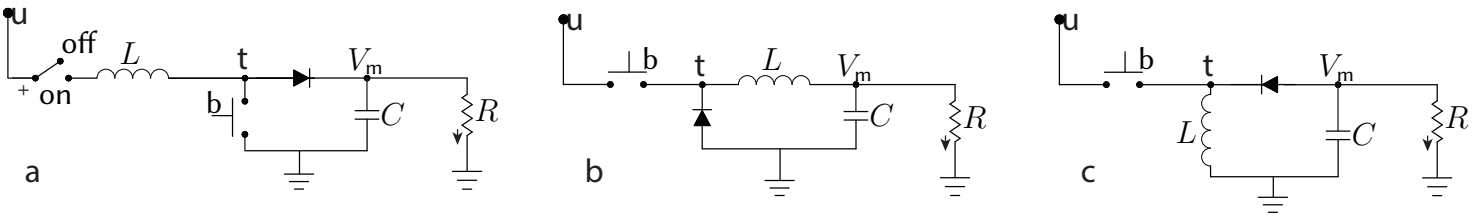


Figure 10.21: Essential components of a boost converter.

Example 10.20 Boost converters. Boost converters are used for DC-to-DC voltage conversion, to step from a given V_{in} up to a higher output voltage V_{out}. The essential components of these devices are illustrated in Figure 10.21. For the purpose of analysis, we assume this circuit is initialized, up to time $t = 0$, with the switch at left in the **off** position, and with $V_{\text{in}} = V_{\text{m}} = V_{\text{out}} = 0$.

Startup. At time $t = 0$, the switch at left is moved to the ON position, thus setting $V_{\text{in}} = V_s$ (the constant voltage of the ideal voltage source); the button b is left open (as shown). Denote positive current through the inductor, capacitor, and the resistor (aka the "load"), in the directions indicated, as I_L, I_C, and I_R, respectively.

Assume the voltage drop of the diode d, under forward bias, is V_d (another constant, with $V_d \ll V_s$), so that the moment that current starts flowing, at $t = 0$, V_m jumps up to V_d. Thereafter, the eqn for the diode, while it remains under forward bias, is simply $V_{\text{m}} - V_{\text{out}} = V_d$. Combining with the other three component eqns, and the KCL eqn at the V_{out} node, we thus have 5 total eqns in the 5 variables $\{I_L(t), I_C(t), I_R(t), V_{\text{m}}(t), V_{\text{out}}(t)\}$ [note that the current through the diode is just I_L]. Our 5 eqns are thus

$$V_s - V_{\text{m}}(t) = L\, d[I_L(t)]dt,\ V_{\text{m}}(t) - V_{\text{out}}(t) = V_d,\ I_C(t) = C\, d[V_{\text{out}}(t)]/dt,\ V_{\text{out}}(t) = R\, I_R(t),\ I_L(t) = I_C(t) + I_R(t),$$

which may be Laplace transformed and rearranged such that

$$I_L(s) = [V_s - V_{\text{m}}(s)]/(s\, L),\ V_{\text{m}}(s) = V_{\text{out}}(s) + V_d,\ I_C(s) = s\, C\, V_{\text{out}}(s),\ I_R(s) = V_{\text{out}}(s)/R,\ I_L(s) = I_C(s) + I_R(s).$$

Combining these 5 eqns (starting from the KCL) to eliminate $\{I_L(s), V_{\text{m}}(s), I_C(s), I_R(s)\}$ gives

$$\begin{aligned} & \{V_s - [V_{\text{out}}(s) + V_d]\}/(s\, L) = s\, C\, V_{\text{out}}(s) + V_{\text{out}}(s)/R \\ \Rightarrow \quad & R\,[V_s - V_d - V_{\text{out}}(s)] = s^2\, R\, L\, C\, V_{\text{out}}(s) + s\, L\, V_{\text{out}}(s) \\ \Rightarrow \quad & (s^2\, R\, L\, C + s\, L + R)\, V_{\text{out}}(s) = R\,(V_s - V_d). \end{aligned} \tag{10.13a}$$

Combine the last 3 eqns (again, starting from the KCL) gives

$$I_L(s) = s\, C\, V_{\text{out}}(s) + V_{\text{out}}(s)/R \quad \Rightarrow \quad I_L(t) = (C\, d/dt + 1/R) V_{\text{out}}(t); \tag{10.13b}$$

once we solve (10.13a) for $V_{\text{out}}(t)$, we can just substitute the result into (10.13b) to determine $I_{\text{L}}(t)$.

Take the Laplace transform of these eqns, denoting (for convenience later, in problem [3]) the initial value of $I_L(t)$ as I_L^B, and the initial value of V_{out} as V_{out}^B. Combine these 5 algebraic eqns to determine a single algebraic eqn for $V_{\text{out}}(s)$. Combine these eqns in a different way to determine a single algebraic eqn for $I_L(s)$.

Since $V_m(t) - V_{\text{out}}(t) = 0$ for $t \leq 0$, and $V_m(t) - V_{\text{out}}(t) = V_d$ for $t > 0$, we may write

$$V_m(s) - V_{\text{out}}(s) = V_d/s. \tag{10.14a}$$

Taking this relation together with the three component eqns (for the resistor, capacitor, and inductor, noting similarly that $V_{\text{in}}(t) = 0$ for $t < 0$ and $V_{\text{in}}(t) = V_s$ for $t \geq 0$, and thus $V_{\text{in}}(s) = V_s/s$), as well as the KCL relation at the V_{out} node, once taking their Laplace transform, we arrive at 5 algebraic eqns in the 5 variables

$\{I_L(s), I_C(s), I_R(s), V_{\rm m}(s), V_{\rm out}(s)\}$. Denoting (for later convenience) the initial value of $I_L(t)$ as I_L^B, and the initial value of $V_{\rm out}$ as $V_{\rm out}^B$, the other 4 eqns in this set (3 component eqns and 1 KCL) may be written

$$V_{\rm out}(s) = R\, I_R(s), \;\; I_C(s) = C\,[sV_{\rm out}(s) - V_{\rm out}^B], \;\; V_s/s - V_{\rm m}(s) = L\,[sI_L(s) - I_L^B], \;\; I_L = I_C + I_R. \quad (10.14b)$$

The 5 eqns in (10.14) may be combined to determine stand-alone algebraic eqns for $V_{\rm out}(s)$ and $I_L(s)$, as shown in the corresponding code in RR Chapter 10, which gives immediately:

$$V_{\rm out}(s) = \frac{b_2\, s^2 + b_1\, s + b_0}{s\,[s^2 + a_1 s + a_0]}, \quad I_L(s) = \frac{c_2\, s^2 + c_1\, s + c_0}{s\,[s^2 + a_1 s + a_0]}, \quad \text{where} \quad a_1 = 1/(C\,R), \quad a_0 = 1/(L\,C) \quad (10.15)$$
$$b_2 = V_{\rm out}^B, \quad b_1 = I_L^B/C, \qquad\qquad b_0 = (V_s - V_d)/(L\,C),$$
$$c_2 = I_L^B, \quad c_1 = (V_s - V_d - V_{\rm out}^B)/L + I_L^B/(C\,R), \quad c_0 = (V_s - V_d)/(L\,C\,R).$$

Noting the $e^{-\sigma t}\cos(\omega_d t)$ and $e^{-\sigma t}\sin(\omega_d t)$ entries in Table 9.1, and setting $\sigma = a_1/2$, and $\omega_d = \sqrt{a_0 - a_1^2/4}$, we may rewrite (10.15) as

$$V_{\rm out}(s) = \frac{b_2\, s^2 + b_1\, s + b_0}{s\,[s^2 + a_1 s + a_0]} = \frac{b_2\, s^2 + b_1\, s + b_0}{s\,[(s+\sigma)^2 + \omega_d^2]} = B_2\,\frac{1}{s} + B_1\frac{(s+\sigma)}{(s+\sigma)^2 + \omega_d^2} + B_0\frac{\omega_d}{(s+\sigma)^2 + \omega_d^2}. \quad (10.16a)$$

$$I_L(s) = \frac{c_2\, s^2 + c_1\, s + c_0}{s\,[s^2 + a_1 s + a_0]} = \frac{c_2\, s^2 + c_1\, s + c_0}{s\,[(s+\sigma)^2 + \omega_d^2]} = C_2\,\frac{1}{s} + C_1\frac{(s+\sigma)}{(s+\sigma)^2 + \omega_d^2} + C_0\frac{\omega_d}{(s+\sigma)^2 + \omega_d^2}. \quad (10.16b)$$

This may be solved for $\{B_2, B_1, B_0\}$ and $\{C_2, C_1, C_0\}$ by forming a common denominator and setting like powers of s in the numerator as equal, as shown previously, which gives

$$B_2 = \frac{b_0}{\sigma^2 + \omega_d^2}, \;\; B_1 = b_2 - B_2, \;\; B_0 = \frac{b_1 - b_2\sigma}{\omega_d} - B_2\frac{\sigma}{\omega_d}, \;\; C_2 = \frac{c_0}{\sigma^2 + \omega_d^2}, \;\; C_1 = c_2 - C_2, \;\; C_0 = \frac{c_1 - c_2\sigma}{\omega_d} - C_2\frac{\sigma}{\omega_d},$$

and thus, for $t \geq 0$

$$V_{\rm out}(t) = B_2 + B_1\, e^{-\sigma t}\cos(\omega_d\, t) + B_0\, e^{-\sigma t}\sin(\omega_d\, t), \quad I_L(t) = C_2 + C_1\, e^{-\sigma t}\cos(\omega_d\, t) + C_0\, e^{-\sigma t}\sin(\omega_d\, t), \quad (10.17)$$

where the constants $\{\omega_d, \sigma, B_2, B_1, B_0, C_2, C_1, C_0\}$ depend on $\{L, C, R, V_s, V_d, V_{\rm out}^B, I_L^B\}$ via the equations above.

It follows from (10.17) that $V_{\rm out}(t=0) = B_2 + B_1 = b_2 = V_{\rm out}^B$ and $I_L(t=0) = C_2 + C_1 = c_2 = I_L^B$, as specified. Thus, simplifying (10.17) by taking $V_{\rm out}^B = I_L^B = 0$ gives $V_{\rm out}(t=0) = I_L(t=0) = 0$, as expected. Both $V_{\rm out}(t)$ and $I_L(t)$ are oscillating decaying sinusoids with frequency $\omega_d = \sqrt{1/(L\,C) - 1/(4\,C^2\,R^2)}$ and damping $\sigma = 1/(2\,C\,R)$, eventually approaching $V_{\rm out}(t) \to B_2 = V_s - V_d$ and $I_L(t) \to C_2 = (V_s - V_d)/R$.

If the diode is removed (thus setting $V_d = 0$ in our equations), the above expressions would apply for all $t \geq 0$. With the diode present, this solution is only valid until $I_L(t)$ falls to zero, after which time the diode shuts off. However, taking $V_{\rm out}^B = I_L^B = 0$ and finite positive values for $\{L, C, R\}$, $I_L(t) > 0$ for all $t \geq 0$, so the above solution is valid for all $t \geq 0$ in the setting described as long as the button b is not pressed.

Phase A. At time $t = t_A$, the button b is pressed **closed** (leaving the switch at left in the **on** position); the moment this button is pressed, V_m jumps down to 0 (that is, to GND). Thus, by pressing this button, the diode is put under reverse bias, effectively isolating the portion of the circuit to the left of the diode from that to its right. These two portions of the circuit, now electrically isolated, are thus analyzed separately below.

The current $I_L(t)$ for $t_A \leq t \leq t_B$ is governed by a single ODE, with an initial value at $t = t_A$ of I_L^A, which may be solved as follows:

$$dI_L(t)/dt = V_s/L \;\; \text{with} \;\; I_L(t_A) = I_L^A \;\; \Rightarrow \;\; \boxed{I_L(t) = V_s(t - t_A)/L + I_L^A \;\; \text{for} \;\; t_A \leq t \leq t_B.}$$

The voltage $V_{\text{out}}(t)$ for $t_A \le t \le t_B$ is also governed by a single ODE, with an initial value at $t = t_A$ of V_{out}^A, which may be solved as follows:

$$[1/(RC) + d/dt]\, V_{\text{out}}(t) = 0 \quad \text{with} \quad V_{\text{out}}(t_A) = V_{\text{out}}^A \quad \Rightarrow \quad \boxed{V_{\text{out}}(t) = V_{\text{out}}^A\, e^{-(t-t_A)/(RC)} \quad \text{for} \;\; t_A \le t \le t_B.}$$

Phase B. At time $t = t_B$, the button b is released to **open** (leaving the switch at left in the **on** position); the moment the button is released, the current from the inductor is again rerouted through the diode, and V_m jumps back up to again satisfy the equation $V_{\text{m}} - V_{\text{out}} = V_d$. The voltage and current of this circuit are thus precisely as given in (10.17) in the vicinity of $t' = t - t_B = 0$, with nonzero initial values, at $t' = 0$ (that is, at $t = t_B$), of I_L^B and V_{out}^B, determined by evaluating the boxed expressions above for $I_L(t)$ and $V_{\text{out}}(t)$ at $t = t_B$:

$$\boxed{\begin{aligned} V_{\text{out}}(t) &= B_2 + B_1\, e^{-\sigma(t-t_B)} \cos[\omega_d\,(t-t_B)] + B_0\, e^{-\sigma(t-t_B)} \sin[\omega_d\,(t-t_B)] \quad \text{for} \;\; t_B \le t \le t_C \\ I_L(t) &= C_2 + C_1\, e^{-\sigma(t-t_B)} \cos[\omega_d\,(t-t_B)] + C_0\, e^{-\sigma(t-t_B)} \sin[\omega_d\,(t-t_B)] \quad \text{for} \;\; t_B \le t \le t_C. \end{aligned}}$$

Periodic oscillation. At time $t = t_C$, the button b is again pressed **closed** (again, leaving the switch at left in the **on** position), thus re-entering Phase A, with nonzero initial values for I_L^A and V_{out}^A, determined by evaluating the expressions above for $V_{\text{out}}(t)$ and $I_L(t)$ at $t = t_C$. Replacing the button with a MOSFET connected to GND, and excited at its gate with a PWM signal (generated by a microcontroller, like that on the Berets in §5), this process repeats periodically, at a constant (very high) frequency f and duty cycle D where $0 < D < 1$, for some t_A and corresponding $t_B = t_A + D/f$ and $t_C = t_A + 1/f$. After repeating many times, a periodic behavior of the circuit settles in over each period $t_A \leq t \leq t_C$ (that is, at the same frequency f as this PWM excitation).

The periodic condition that this system converges to may be found by setting the values of $I_L(t)$ and $V_{\text{out}}(t)$ at $t = t_A$ equal to the values of $I_L(t)$ and $V_{\text{out}}(t)$ at $t = t_C$ in the above analysis. Evaluating the first two boxed equations at time $t = t_B$, setting $V_{\text{out}}(t_B) = V_{\text{out}}^B$ and $I_L(t_B) = I_L^B$, and the second two boxed equations at time $t = t_C$, setting $V_{\text{out}}(t_C) = V_{\text{out}}^A$ and $I_L(t_C) = I_L^A$, gives four conditions for this periodic behavior, which may then be solved to find the $\{V_{\text{out}}^A, V_{\text{out}}^B, I_L^A, I_L^B\}$ which simultaneously solve these four equations:

$$V_{\text{out}}^B = V_{\text{out}}^A \, e^{-(t_B - t_A)/(RC)}, \tag{10.18a}$$

$$I_L^B = V_s(t_B - t_A)/L + I_L^A, \tag{10.18b}$$

$$V_{\text{out}}^A = B_2 + B_1 \, e^{-\sigma(t_C - t_B)} \cos[\omega_d \, (t_C - t_B)] + B_0 \, e^{-\sigma(t_C - t_B)} \sin[\omega_d \, (t_C - t_B)], \tag{10.18c}$$

$$I_L^A = C_2 + C_1 \, e^{-\sigma(t_C - t_B)} \cos[\omega_d \, (t_C - t_B)] + C_0 \, e^{-\sigma(t_C - t_B)} \sin[\omega_d \, (t_C - t_B)], \tag{10.18d}$$

where

$$\omega_d = \sqrt{1/(L\,C) - 1/(4\,C^2\,R^2)}, \quad \sigma = 1/(2\,C\,R), \quad t_B - t_A = D/f, \quad t_C - t_B = (1-D)/f = \bar{D}/f,$$

$$B_2 = V_s - V_d, \qquad B_1 = V_{\text{out}}^B - (V_s - V_d), \qquad B_0 = [I_L^B/C - V_{\text{out}}^B \sigma]/\omega_d - B_2\sigma/\omega_d,$$

$$C_2 = (V_s - V_d)/R, \quad C_1 = I_L^B - (V_s - V_d)/R, \quad C_0 = [(V_s - V_d - V_{\text{out}}^B)/L + I_L^B(\sigma - 1/(C\,R))]/\omega_d - C_2.$$

The equations above are easily typed directly into the computer and solved, as done in the corresponding code in RR Chapter 10), to give $\{V_{\text{out}}^A, V_{\text{out}}^B, I_L^A, I_L^B\}$ as complicated functions of $\{V_s, V_d, L, C, R, f, D\}$. Note that the expressions are generally too involved to determine reliably by hand.

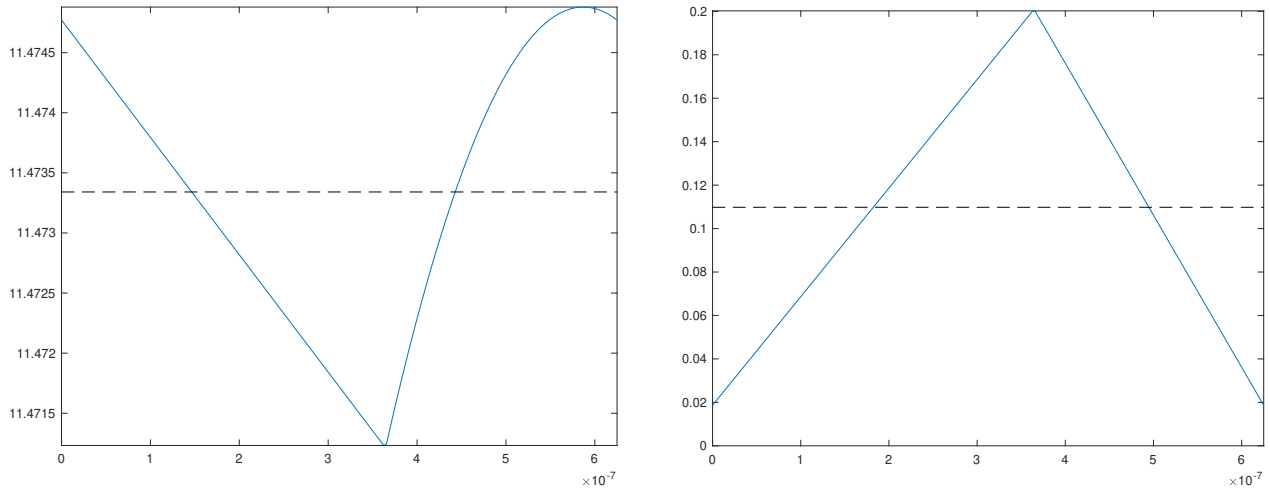


Figure 10.22: Representative curves for (left) $V_{\text{out}}(t)$ and (right) $I_L(t)$ over $t_A \leq t \leq t_C$ for a boost converter.

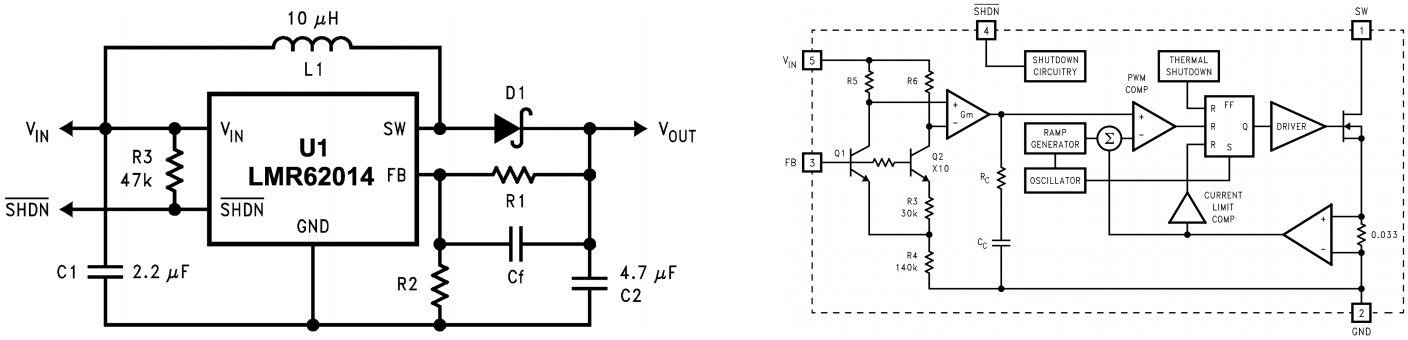


Figure 10.23: The (left) external wiring and (right) internal circuitry of the TI LMR62014.

Given the values of $\{I_L^A, V_{\text{out}}^A, I_L^B, V_{\text{out}}^B, I_L^C, V_{\text{out}}^C\}$ characterizing the periodic oscillations (with $I_L^A = I_L^C$ and $V_{\text{out}}^A = V_{\text{out}}^C$) as determined above, taking $V_s = 5\,\text{V}$, $V_d = 0.5\,\text{V}$, $L = 10\,\mu\text{H}$, $C = 4.7\,\mu\text{F}$, $R = 250$ ohms, $f = 1.6\,\text{MHz}$, and $D = 7/12$, and noting the four boxed equations above for $V_{\text{out}}(t)$ and $I_L(t)$ over both Phase A ($t_A \leq t < t_B$) and Phase B ($t_B \leq t < t_C$), the corresponding $V_{\text{out}}(t)$ and $I_R(t)$ are plotted over the entire interval $t_A \leq t \leq t_C$ in Figure 10.22. Note that V_{out} is a decaying exponential on (t_A, t_B), and a decaying sinusoid on (t_B, t_C); I_L is linear on (t_A, t_B), and a decaying sinusoid on (t_B, t_C). When excited at a high frequency f, most of these curves appear to be nearly linear over each phase. Overall, there are relatively small fluctuations in $V_{\text{out}}(t)$, and relatively large fluctuations in $I_L(t)$. Note also that $I_L^{\text{mean}} \approx V_{\text{out}}^{\text{mean}}/[R\,(1-D)]$. By trial and error, it is found that a slightly adjusted value of $D \approx 0.60086$ gives $V_{\text{out}}^{\text{mean}} \approx 12V$.

Implementation. Rather than running at a fixed duty cycle, *feedback* can be implemented to identify the duty cycle D required to more precisely achieve a desired value of $V_{\text{out}}^{\text{mean}}$. This is especially important when the value of V_{in} is not accurately known (e.g., if it comes from the output of a LiPo, which ranges from 3.0 to 4.2 V per cell). This may be achieved, e.g., by implementing a TI LMR62014, which is compact (less than $9\,\text{mm}^2$), easy to hook up (SMT, 5 pins), and inexpensive ($0.27). The (simple) external wiring and (complicated) internal circuitry diagrams for the LMR62014 (which generates the required PWM signal with a few op amps) are illustrated in Figure 10.23; note that $\{L, d, C\}$ in Figure 10.21 correspond to $\{L1, D1, C2\}$ in the external wiring diagram (Figure 10.23a), and the button b is replaced by a PWM-actuated MOSFET illustrated near the right side of the internal circuitry diagram (Figure 10.23b). $V_{\text{out}}(t)$ may then be hooked to a load of a few hundred ohms, and this circuit will drive the tens of mA necessary to drive this load. Note also that the $I_L(t)$ plot given in Figure 10.22 also appears on page 12 of the LMR62014 datasheet.

Example 10.21 Buck-boost converters.

A buck-boost converter, as illustrated in Figure **??**c, is capable of stepping an input DC voltage either up or down, as necessary, to generate a well-regulated output voltage. The essential circuit design of a buck-boost converter is illustrated in Figure **??**.

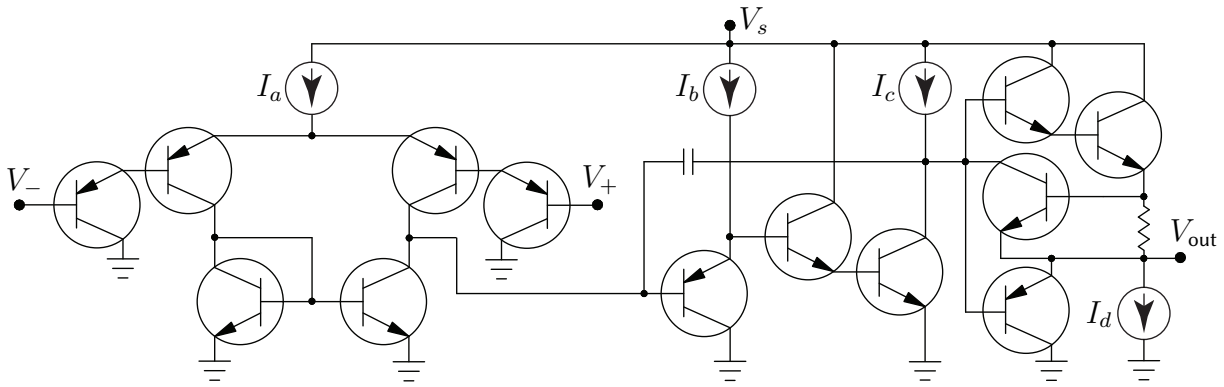


Figure 10.24: Internal construction of an LM324 op amp, with $I_a = I_b = 6\,\mu$A, $I_c = 100\,\mu$A, $I_d = 50\,\mu$A. The first stage of the op amp is the differential amplifier considered in Example 10.17 (see Figure 10.17c), with **darlington transistors** (that is, a cascade of two transistors, interconnected as shown) used on each of the inputs to increase the gain, and the output resistor replaced by the op amp's second stage. The rest of the circuit amplifies the output from the first stage, effectively implements an RC first-order low-pass filter (note the resistor and the capacitor) to suppress very-high-frequency noise, and provides high current driving capability with low output impedance as well as short circuit protection. The LM324 quad op amp implements four such circuits together in a single, robust, and convenient 14-pin **dual in-line package** (**DIP**).

10.3 Operational amplifiers

An **operational amplifier** (a.k.a. **op amp**) is an **active** (powered) integrated circuit with two inputs, $V_+(t)$ and $V_-(t)$, and one output, $V_{\text{out}}(t)$, that functions as a differential amplifier with output

$$V_{\text{out}}(t) = \begin{cases} V_{s+} & \text{if } V_{s+} < V_o(t) \\ V_o(t) & \text{if } V_{s-} < V_o(t) < V_{s+} \\ V_{s-} & \text{if } V_o(t) < V_{s-} \end{cases} \quad \text{with} \quad V_o(t) \approx A\,[V_+(t) - V_-(t)], \tag{10.19a}$$

where the gain A is *very* large (indeed, it is often approximated as $A \to \infty$), and two additional properties:

a) **very high input impedance** (that is, the input terminals of the op amp draw negligible current), and
b) **very low output impedance** (that is, the output voltage of the op amp is set by the input voltages as specified above, essentially independent of the attached load).

The internal construction of an op amp is a fairly involved arrangement of transistors and other circuit elements, as typified by[26] the LM324 op amp illustrated[27] in Figure 10.24. A more accurate *dynamic* model of $V_o(t)$ in the (typical) LM324 op amp, which takes into account the fact that the magnitude of its frequency response rolls off at a couple hundred kilohertz [cf. (10.19a)], may be written in transfer-function form as

$$V_o(s) = G(s)\,[V_+(s) - V_-(s)] \quad \text{with} \quad G(s) = A\,\frac{a}{s+a}, \tag{10.19b}$$

where $A \approx 10^5$ and $a \approx 10^6$. Note that the low-pass-filter nature of an op amp is usually neglected [see (10.19a)]; that is, the cutoff frequency a is so large that the transfer function $G(s)$ of the op amp is usually approximated as a pure gain (and, further, the gain A of an op amp is so large that it is often considered to be essentially infinite when modeling the behavior of an op amp circuit). However, the more precise model of an

[26] Note that there are many such op amp designs that lead to the same essential properties.
[27] Note that, in Figure 10.24, V_{s+} is denoted V_s, and V_{s-} is denoted by ground. Both conventions are common.

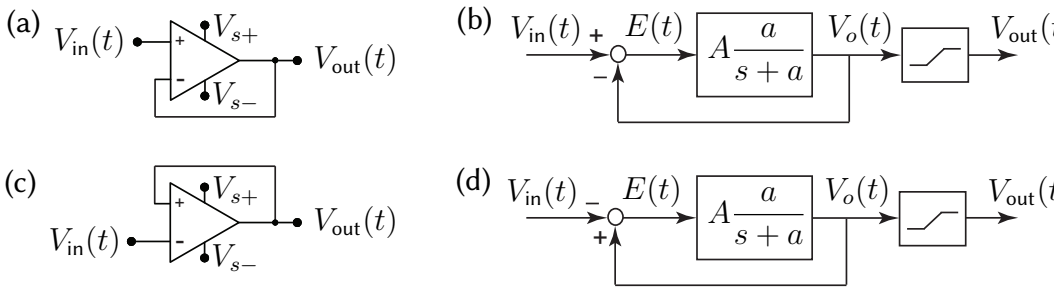


Figure 10.25: Two simple op amp circuits: (a) an op amp wired with negative feedback and (b) its corresponding block diagram, and (c) an op amp wired with positive feedback and (d) its corresponding block diagram. As op amps are **active** devices, their connections to V_{s+} & V_{s-} are often shown explicitly in the op amp symbol, as in (a) and (c); these connections are suppressed for notational simplicity in most of the remainder of this text.

op amp given in (10.19b) is the best starting point to understand op amp behavior, as it explains why an op amp with feedback is either stable or unstable (note that both modes have their uses), depending on which input terminal the feedback is connected to, as shown below.

Consider first the simple op amp circuit in Figure 10.25a, with **negative feedback**, and its corresponding block diagram in Figure 10.25b, with an input-output transfer function of

$$\left.\begin{array}{l} V_o(s) = G(s)\,E(s) \\ E(s) = V_{\text{in}}(s) - V_o(s) \end{array}\right\} \quad \Rightarrow \quad H(s) = \frac{V_o(s)}{V_{\text{in}}(s)} = \frac{G(s)}{1+G(s)} = \frac{aA}{s+a+aA} \approx \frac{aA}{s+aA}.$$

The gain of this first-order low-pass filter is nearly unity over a very wide range of frequencies; note the fast stable pole at $s \approx -aA$. With large A, this circuit behaves as a **voltage follower** or **buffer**, with $V_{\text{out}}(t) \approx V_{\text{in}}(t)$. This active circuit is useful because, due to its high input impedance and low output impedance, it **isolates** the circuits hooked to its input and output terminals; that is, it draws negligible current from the circuit connected to its input terminal, and maintains $V_{\text{out}}(t) \approx V_{\text{in}}(t)$ while providing as much current as required (within limits) by the circuit connected to its output terminal, thus allowing filters to be constructed and analyzed as independent stages then cascaded together, effectively relaxing the restrictive assumptions of Example 10.2.

Now consider the op amp circuit in Figure 10.25c, with **positive feedback**, and its corresponding block diagram in Figure 10.25d, with an input-output transfer function of

$$\left.\begin{array}{l} V_o(s) = G(s)\,E(s) \\ E(s) = V_o(s) - V_{\text{in}}(s) \end{array}\right\} \quad \Rightarrow \quad H(s) = \frac{V_o(s)}{V_{\text{in}}(s)} = \frac{-G(s)}{1-G(s)} = \frac{-aA}{s+a-aA} \approx \frac{-aA}{s-aA}.$$

Due to the (fast) unstable pole at $s = aA$, *the equilibrium $V_o(t) \approx V_{in}(t)$ is unstable*, and is thus, in practice, never realized. Instead, $V_{\text{out}}(t)$ is driven to one of the limiting values of the op amp, V_{s+} or V_{s-}, and stays there; which limit it goes to depends on the initial values of $V_o(t)$ and $V_{\text{in}}(t)$ when the op amp is turned on.

10.3.1 Design and analysis of a few useful op amp circuits

We now show via several examples how the arrangement of transistors in an op amp is convenient in a variety of practical situations. Note that *almost all useful op amps circuits implement feedback*, with Example 10.22 being a notable exception. Further, *almost all useful op amps circuits implementing feedback use the (stable)* **negative feedback** *configuration* discussed above, with Examples 10.25, 10.28, and 10.29 being notable exceptions.

Example 10.22 Voltage comparator. When implemented without feedback, a bare op amp (10.19a) in the large gain limit $A \to \infty$ functions simply as a **voltage comparator**:

$$V_{\text{out}}(t) = \begin{cases} V_{s+} & \text{if } V_+(t) > V_-(t), \\ V_{s-} & \text{if } V_+(t) < V_-(t). \end{cases}$$

Example 10.23 Inverting and noninverting amplifiers. Implementing (stabilizing) feedback to the inverting input of the op amp, an **inverting amplifier** may be implemented as shown in Figure 10.26a, in which

$$V_{\text{in}}(t) - V_-(t) = I_{\text{in}}(t)\, R/M, \quad V_-(t) - V_{\text{out}}(t) = I_R(t)\, R, \quad I_{\text{in}}(t) = I_R(t);$$

applying (10.19b) thus leads to

$$V_{\text{out}}(s) = \frac{a\,A}{s+a}\,[0 - V_-(s)] \quad \Rightarrow \quad \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{-M\,a\,A}{(M+1)s + [a\,A + a(M+1)]} \quad \underset{A\to\infty}{\Longrightarrow} \quad V_{\text{out}}(t) \approx -M\,V_{\text{in}}(t).$$

Similarly, a **noninverting amplifier** may be implemented as shown in Figure 10.26b, in which

$$V_-(t) = I_O(t)\, R/f, \quad V_-(t) - V_{\text{out}}(t) = I_R(t)\, R, \quad I_O(t) = -I_R(t);$$

applying (10.19b) leads to

$$V_{\text{out}}(s) = \frac{a\,A}{s+a}\,[V_{\text{in}}(s) - V_-(s)] \quad \Rightarrow \quad \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{a\,A}{s + a + a\,A/(1+f)} \quad \underset{A\to\infty}{\Longrightarrow} \quad V_{\text{out}}(t) \approx (1+f)\,V_{\text{in}}(t).$$

As illustrated by both of these examples, the (stabilizing) feedback to the inverting input of the op amp leads, in the $A \to \infty$ limit, to the condition that $V_+ = V_-$; note in both cases the very fast stable poles. It often simplifies the analysis of a stable op amp circuit to simply apply the condition $V_+ = V_-$ at the outset; if you have doubts whether or not the circuit considered is stable, implement (10.19b) instead, as done above.

Example 10.24 A general op amp circuit for adding and subtracting. Appropriate combination of the inverting and noninverting amplifiers of Example 10.23 leads to an op amp circuit such that

$$V_{\text{out}}(t) = \sum_{j=1}^{n} m_j\, v_j - \sum_{j=1}^{N} M_j\, V_j, \tag{10.20}$$

that is, to an op amp circuit that can perform an arbitrary linear combination of $n + N$ inputs, with n positive coefficients m_j and N negative coefficients $(-M_j)$. Defining $f = \sum m_j - \sum M_j - 1$, we will consider three cases: $f < 0$, $f = 0$, and $f > 0$. In the sample circuit we will consider, we take $n = N = 3$; the modifications required to handle a different numbers of inputs are trivial. Most op amp circuits used for adding and subtracting, as found online, are special cases of the general circuit presented here.

The circuit required in the $f < 0$ case is illustrated in Figure 10.26c. For notational clarity, in this example only, we take the voltages, currents, and resistances in the upper half of the circuit as uppercase, and the voltages, currents, and resistances in the lower half of the circuit as lowercase. Ohm's law and KCL then give

$$\begin{array}{lllll} V_1 - V_- = I_1\, R/M_1, & V_2 - V_- = I_2\, R/M_2, & V_3 - V_- = I_3\, R/M_3, & V_- - V_{\text{out}} = I_R\, R, & I_1 + I_2 + I_3 = I_R, \\ v_a - v_+ = i_a\, r/m_a, & v_b - v_+ = i_b\, r/m_b, & v_c - v_+ = i_c\, r/m_c, & v_+ = i_o\, r/|f|, & i_a + i_b + i_c = i_o. \end{array}$$

Since negative (stable) feedback is used, assuming $A \to \infty$, we take $V_- = v_+$; noting that $f = \sum m_j - \sum M_j - 1$ and solving then leads immediately to (10.20).

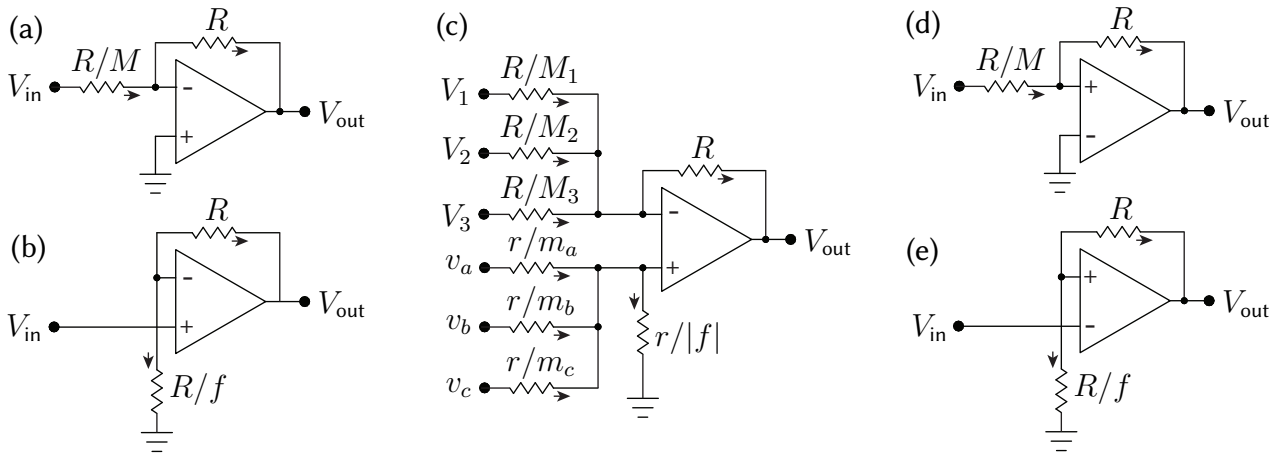


Figure 10.26: Some useful op amp circuits. (a) Inverting amplifier. (b) Noninverting amplifier. (c) A general adder/subtractor [note: the ground connection shown is for $f < 0$; if $f = 0$, this connection to ground is removed; if $f > 0$, the connection to ground is attached to V_- instead of V_+, through a resistance R/f]. (d) Inverting Schmitt trigger. (e) Noninverting Schmitt trigger. Note that (d) and (e) are hysteretic.

As $f \to 0$, the resistance of the connection between the noninverting input of the op amp and ground in Figure 10.26c goes to infinity. In the $f = 0$ case, this connection may thus be eliminated entirely; removing the equation $v_+ = i_o\, r/|f|$ from the above set of equations, taking $i_o = 0$, and solving leads again to (10.20).

Finally, in the $f > 0$ case, we replace the connection between the noninverting input of the op amp and ground with a connection between the inverting input of the op amp and ground, with resistance R/f. In this case, the equation $v_+ = i_o\, r/|f|$ in the above set of equations is replaced by $V_- = I_o\, R/f$, and the two KCL relations are now $I_1 + I_2 + I_3 = I_o + I_R$ and $i_a + i_b + i_c = 0$; solving again leads to (10.20).

In all three cases, $f < 0$, $f = 0$, and $f > 0$, the resulting relation between the voltages, (10.20), is in fact *independent* of both R and r, which are typically selected so that all resistors used in the circuit are between 1 kΩ and 100 kΩ. Note that, in the case that $n = 0$ (see, e.g., Figure 10.26a), we may take $r = 0$, wiring the noninverting input of the op amp directly to ground. In the case that $n = 1$ and $f \geq 0$ (see, e.g., Figure 10.26b), we may also take $r = 0$, wiring the noninverting input of the op amp directly to v_a.

Example 10.25 Schmitt triggers. We now consider two **hysteretic** circuits that are simply the inverting and noninverting amplifiers of Example 10.23 with the inputs to the op amp swapped from the stable (negative-feedback) configuration to the unstable (positive-feedback) configuration. Assuming $V_{s+} = V_s$ and $V_{s-} = -V_s$,

- in the unstable circuit illustrated in Figure 10.26d, called a **noninverting Schmitt trigger**,
  - if $V_{\text{out}} = +V_s$, then it will stay there until V_{in} passes below $-V_s/M$ (that is, until V_+ passes below V_-), after which the output will switch to $V_{\text{out}} = -V_s$, whereas
  - if $V_{\text{out}} = -V_s$, then it will stay there until V_{in} passes above V_s/M (that is, until V_+ passes above V_-), after which the output will switch to $V_{\text{out}} = +V_s$;
- in the unstable circuit illustrated in Figure 10.26e, called a **inverting Schmitt trigger**,
  - if $V_{\text{out}} = +V_s$, then it will stay there until V_{in} passes above $V_s/(1+f)$ (that is, until V_- passes above V_+), after which the output will switch to $V_{\text{out}} = -V_s$, whereas
  - if $V_{\text{out}} = -V_s$, then it will stay there until V_{in} passes below $-V_s/(1+f)$ (that is, until V_- passes below V_+), after which the output will switch to $V_{\text{out}} = +V_s$.

A primary application of Schmitt triggers is **switch debouncing**: once a remotely-operated Schmitt trigger, acting as a switch, is flipped one way, it takes a large change in the input to flip the Schmitt trigger the other way, thus preventing "chatter" of the switch due to noise over the communication channel.

Example 10.26 A general-purpose inverting first-order filter. The circuit illustrated in Figure 10.27a is a remarkably flexible general-purpose inverting first-order filter design with transfer function[28]

$$F(s) = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = -\frac{C_1}{C_2}\,\frac{s+1/(R_1C_1)}{s+1/(R_2C_2)} = -\frac{R_2}{R_1}\,\frac{1+R_1C_1s}{1+R_2C_2s} = -R_2C_1\,\frac{s+1/(R_1C_1)}{1+R_2C_2s} = -\frac{1}{R_1C_2}\,\frac{1+R_1C_1s}{s+1/(R_2C_2)}.$$

That is, $F(s) = -K_0(s+z)/(s+p)$, where $K_0 = C_1/C_2$, $z = 1/(R_1C_1)$, and $p = 1/(R_2C_2)$; we also define $K_1 = R_2/R_1$, $K_2 = R_2C_1$, and $K_3 = 1/(R_1C_2)$. If the op amp is ideal, the circuit design in Figure 10.27a is actually nine circuits in one, reducing[29] in the appropriate limits to *all* of the inverting first-order filters:

- taking $R_1C_1 > R_2C_2$, it is an inverting **lead filter** with $F(s) = -K_0(s+z)/(s+p)$ where $z < p$;
- taking $R_2C_2 > R_1C_1$, it is an inverting **lag filter** with $F(s) = -K_0(s+z)/(s+p)$ where $p < z$;
- removing C_1, it is an inverting **first-order low-pass filter** with $F(s) = -K_3/(s+p)$;
- removing R_1, it is an inverting **first-order high-pass filter** with $F(s) = -K_0\,s/(s+p)$;
- removing[30] R_2, it is an inverting **PI filter** with $F(s) = -K_0\,(s+z)/s$;
- removing[30] R_2 and C_1, it is an inverting **pure integrator** $F(s) = -K_3/s$;
- removing C_2, it is an inverting **PD filter**[31] with $F(s) = -K_2\,(s+z)$;
- removing C_2 and R_1, it is an inverting **pure differentiator**[31] $F(s) = -K_2\,s$;
- removing C_1 and C_2, it is an inverting **amplifier** $F(s) = -K_1$.

The development of a corresponding general-purpose *noninverting* first-order filter is considered in Exercise 10.6. To build a second-order filter that incorporates both a first-order lag filter at low frequencies (to reduce steady-state error) and a first-order lead filter at high frequencies (to improve damping and reduce overshoot), creating what is called a **lead/lag filter** (see Figure ??b), one may simply cascade together the lead and lag filters described above as necessary. Note that a **PID filter** is simply a special case of a lead/lag filter with

- the roll-off of the integral action of the lag filter taken all the way down to $\omega \to 0$, and
- the roll-off of the derivative action of the lead filter taken all the way up to $\omega \to \infty$.

To build a PID filter, one could simply cascade together the PI and PD filters described above. However, note that lead/lag filters are strongly preferred over PID filters for the reasons discussed in §??: that is, the roll-off of the low-frequency gain and the high-frequency gain mentioned above almost never need to be taken all the way to zero and infinity respectively, and doing such generally causes significant problems (specifically, *integrator windup* and the *amplification of high-frequency noise*) in the closed-loop setting.

Example 10.27 Notch filter. The circuit illustrated in Figure 10.27a, called an **active twin-T filter**, is a convenient op amp circuit implementation of the **notch** transfer function[28]

$$F_{\text{notch}}(s) = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = K\,\frac{s^2+\omega_o^2}{s^2+(\omega_o/Q)s+\omega_o^2} \tag{10.21}$$

where[32] $K = 1 + R_2/R_1$, $Q = 1/[2(2-K)]$, and $\omega_o = 1/(RC)$. Note that the zeros of the notch are pure imaginary, and the so-called "**quality**" of the notch is given by $Q = 1/(2\zeta)$, where ζ is the damping of its poles;

[28] This transfer function is easily derived from the corresponding circuit via the techniques used in Examples 10.23 and 10.24.

[29] Note that removing a capacitor corresponds to taking its capacitance $C \to 0$, and removing a resistor corresponds to taking its resistance $R \to \infty$; in both cases, by (10.2), the current goes to zero through the (removed) component regardless of the applied voltage.

[30] Alternatively, R_2 may be replaced by a switch, allowing the integrator to be reset whenever desired.

[31] PD filters and pure differentiators must never be used in practice, because they amplify high-frequency noise without bound, which is a significant problem. *Lead filters* and *first-order high-pass filters* (a.k.a. **dirty differentiators**) should be used instead.

[32] Note that Q and K can not be set independently in this particular circuit; this usually does not create much of issue, however, because a notch filter is usually cascaded with other op amp circuits that can be used to set the gain to the desired value.

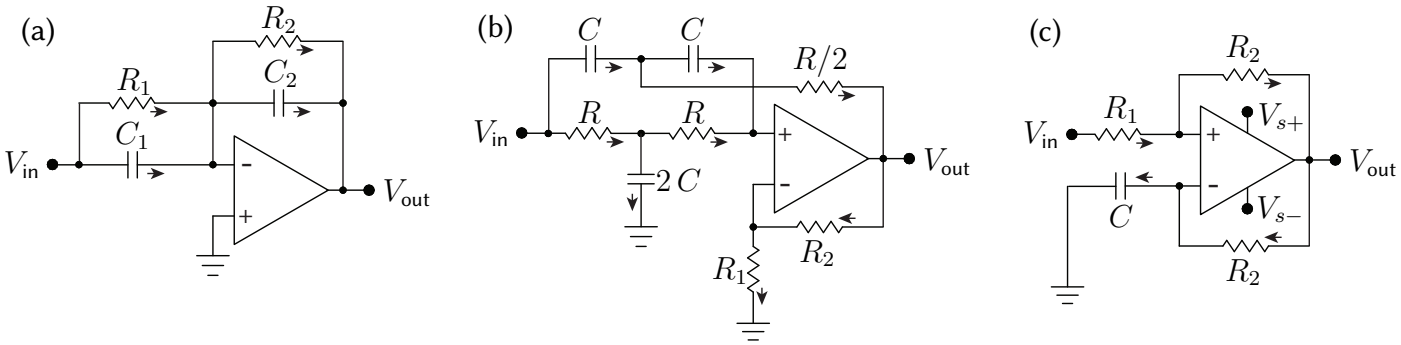


Figure 10.27: Some *dynamic* op amp circuits: (a) an **inverting first-order filter** $F(s) = -K(s+z)/(s+p)$, which may be simplified in various ways; (b) a **notch filter** $F_{\text{notch}}(s) = K(s^2+\omega_o^2)/(s^2+\omega_o\,s/Q+\omega_o^2)$; and (c) a circuit which, taking $V_{\text{in}} = 0$, $V_{s+} = +V_s$, $V_{s-} = -V_s$, and $R_1 = R_2 = R$, gives a square-wave **relaxation oscillator** with frequency $1/(2RC\,\ln 3)$ Hz and duty cycle $1/2$, whereas, taking $V_{s+} = V_s$, $V_{s-} = 0$, and $R_1 \ll R_2$, gives a square wave with duty cycle V_{in}/V_s and frequency $V_{\text{in}}(V_s - V_{\text{in}})/(R_1\,C\,V_s^2)$ Hz, which may be used to drive a load in an efficient partial power setting via a **pulse width modulation** strategy.

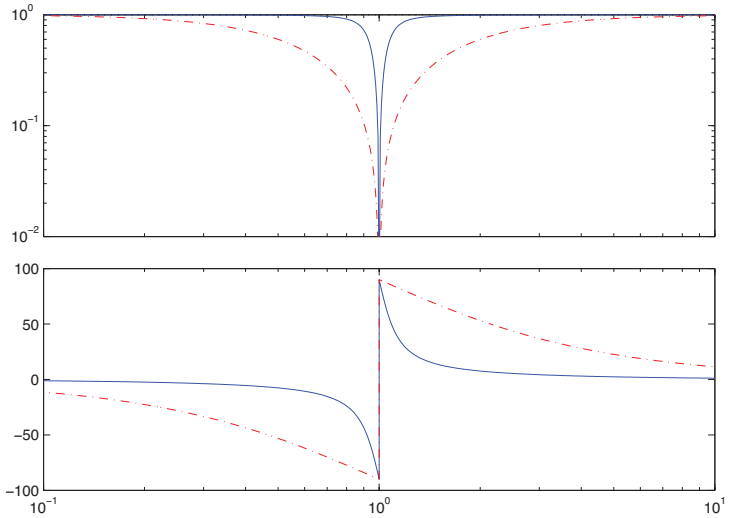


Figure 10.28: Bode plot of the **notch filter** of Example 10.27, rescaled such that $K = 1$, taking $\omega_o = 1$, (dot-dashed) $Q = 0.5$, and (solid) $Q = 5$. Note the "notch" shape of the magnitude part of the Bode plot.

thus, $Q = 0.5$ (that is, $K = 1$, or $R_2 = 0$ and $R_1 \to \infty$) corresponds to two identical real poles, and $Q > 0.5$ corresponds to a pair of complex-conjugate poles with damping which decreases as Q is increased.

The Bode plot of $F_{\text{notch}}(s)$ for $\omega_o = 1$ and two different values of Q is illustrated in Figure 10.28; note that the gain of the notch filter is zero at ω_o, and that the width of the range of frequencies significantly affected by the notch decreases with increasing Q. When using a notch to eliminate, e.g., a 50 or 60 Hz "buzz" (that is, noise with a very narrow power spectrum) in a signal, a high Q value is used to minimize the impact of the notch on the signal of interest outside of the range of frequencies corrupted by the buzz. However, when using a notch in a feedback control setting to "knock out" the oscillatory dynamics of a plant (see §??), one certainly does *not* want to introduce lightly damped poles with the notch, and values of Q in the range $0.5 \le Q \le 0.707$ are preferred[33]. Note finally that an active twin-T implementation of a notch filter may be cascaded with a doubled lead filter to move the poles resulting from the notch even further into the LHP.

[33] That is, when implementing a notch filter to stabilize, e.g., a Ford automobile, achieving high quality is *not* necessarily job one.

Example 10.28 Relaxation oscillator. The operation of the **relaxation oscillator** circuit depicted in Figure 10.27c is analogous to the operation of the Schmitt triggers considered previously, with the successive charging and discharging of a capacitor leading to the periodic flipping of the switch. Assume that $V_{\text{in}} = 0$, $V_{s+} = +V_s$, $V_{s-} = -V_s$, $R_1 = R_2 = R$, and that V_+ is initially higher than V_-. Given this initial state,

(a) $V_{\text{out}} = V_s$, and thus $V_+ = V_s/2$, as the two upper resistors act as a voltage divider. Current thus flows from the output of the op amp through the lower resistor and the capacitor to ground, charging the capacitor until V_- just exceeds $V_+ = V_s/2$, and the switch flips to state (b).

(b) $V_{\text{out}} = -V_s$, and thus $V_+ = -V_s/2$. Current thus flows from ground through the capacitor and the lower resistor to the output of the op amp, charging the capacitor the other direction until V_- falls just below $V_+ = -V_s/2$, and the switch flips back to state (a).

The period of this oscillation is constant, and may be calculated by determining how long it takes the capacitor of the relaxation oscillator to gather sufficient charge to flip the switch in each state. For example, taking $V_{\text{out}} = V_s$ and $V_-(0) = -V_s/2$, the dynamics of state (a) are governed by

$$C\frac{d}{dt}(V_- - 0) = \frac{V_s - V_-}{R} \quad \Rightarrow \quad \Big(1 + RC\,\frac{d}{dt}\Big)V_- = V_s.$$

The homogeneous solution of this system is $V_-(t) = Ae^{-t/(RC)}$, and a particular solution is $V_-(t) = V_s$. Combining and matching the initial condition $V_-(0) = -V_s/2$, the full solution is given by

$$V_-(t) = V_s - (3V_s/2)e^{-t/(RC)}.$$

Setting $V_-(t)$ equal to $V_s/2$ at $t = T/2$, when the switch flips to state (b), it is easy to compute the period T:

$$V_-(T/2) = V_s - (3V_s/2)\,e^{-T/(2RC)} = V_s/2 \quad \Rightarrow \quad e^{-T/(2RC)} = 1/3 \quad \Rightarrow \quad T = 2RC\,\ln 3.$$

Example 10.29 Efficient power control of purely resistive loads via pulse width modulation. Given a power supply (e.g., a battery) and a purely resistive load (e.g., a light bulb), a question arises as to the most effective way to run the load at partial power. An inefficient solution to this problem is simply to put a **variable resistor** (a.k.a. **rheostat**) in series with the load, thus reducing both the current through the load and the voltage across the load, thereby reducing the power consumed by the load. Unfortunately, the variable resistor used in such a setting itself consumes a lot of power that is rejected as waste heat, thereby wiping out any potential energy savings that might otherwise be realized.

A much more efficient way to regulate the power applied to a purely resistive load is to *repeatedly cycle the voltage applied to the load on and off very quickly*; the percentage of the time the switch is on, called the **duty cycle**, then regulates the (time-averaged) percentage of full power at which the load will operate. This solution, referred to as **pulse width modulation** (**PWM**), is facilitated by the fact that transistors are quite efficient when operated as fast switches (see Guideline 10.1).

It is instructive to note that the simple op amp circuit considered in Example 10.28 can in fact be put to task quite easily in the PWM setting. The component relations and KCL in the upper and lower portions of the circuit lead, respectively, to

$$\frac{V_{\text{in}} - V_+}{R_1} = \frac{V_+ - V_{\text{out}}}{R_2} \quad \Rightarrow \quad V_+ = \frac{R_2\,V_{\text{in}} + R_1\,V_{\text{out}}}{R_1 + R_2}, \tag{10.22a}$$

$$C\frac{d}{dt}(V_- - 0) = \frac{V_{\text{out}} - V_-}{R_2} \quad \Rightarrow \quad \Big(1 + R_2\,C\,\frac{d}{dt}\Big)V_- = V_{\text{out}}. \tag{10.22b}$$

Taking $V_{s+} = V_s$, $V_{s-} = 0$, and $R_1 \ll R_2$ and defining the limits $V_{+,\text{max}} = (R_2\,V_{\text{in}} + R_1\,V_s)/(R_1 + R_2)$ and $V_{+,\text{min}} = R_2\,V_{\text{in}}/(R_1 + R_2)$, it follows, as in Example 10.28, that there are two states to consider:

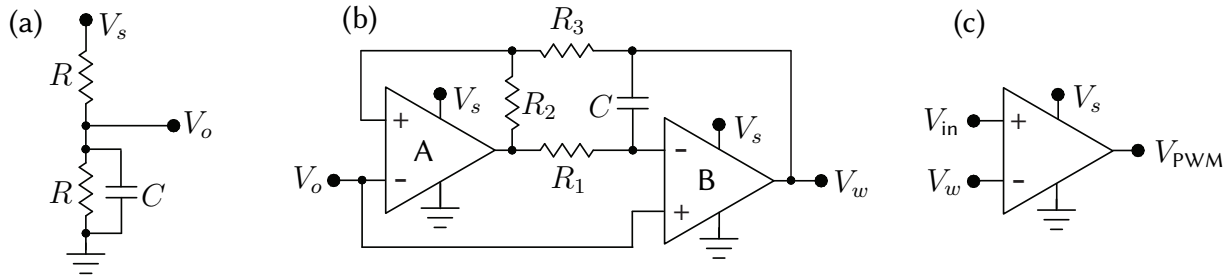


Figure 10.29: An improved PWM circuit with duty cycle V_{in}/V_s and frequency $1/(4\,R_1\,C)$ Hz, formed by the cascade of (a) a passive **stabilized voltage divider**, (b) a **triangle-wave generator**, and (c) a **comparator**.

(a) $V_{\text{out}} = V_s$, and thus $V_+ = V_{+,\text{max}}$. Starting (10.22b) from an initial condition of $V_- = V_{+,\text{min}}$ at $t = 0$, current flows from the output of the op amp through the lower resistor and the capacitor to ground, charging the capacitor until V_- just exceeds V_+; the switch thus flips to state (b) at time $t = T_1$, which may be computed as follows:

$$V_-(t) = V_s + (V_{+,\text{min}} - V_s)e^{-t/(R_2C)}, \quad V_-(T_1) = V_{+,\text{max}} \quad \Rightarrow$$
$$e^{T_1/(R_2C)} = \frac{V_{+,\text{min}} - V_s}{V_{+,\text{max}} - V_s} = 1 + \frac{R_1}{R_2}\frac{V_s}{(V_s - V_{\text{in}})} \quad \Rightarrow \quad T_1 = R_2\,C\,\ln\left(1 + \frac{R_1}{R_2}\,\frac{V_s}{V_s - V_{\text{in}}}\right) \approx R_1 C \frac{V_s}{V_s - V_{\text{in}}}.$$

(b) $V_{\text{out}} = 0$, and thus $V_+ = V_{+,\text{min}}$. Starting (10.22b) from an initial condition of $V_- = V_{+,\text{max}}$ at $t = 0$ (resetting the time variable t appropriately to simplify the analysis), current flows from ground through the capacitor and the lower resistor to the output of the op amp, discharging the capacitor until V_- falls just below V_+; the switch thus flips back to state (a) at $t = T_2$, which may be computed as follows:

$$V_-(t) = 0 + (V_{+,\text{max}} - 0)e^{-t/(R_2C)}, \quad V_-(T_2) = V_{+,\text{min}} \quad \Rightarrow$$
$$e^{T_2/(R_2C)} = \frac{V_{+,\text{max}}}{V_{+,\text{min}}} = 1 + \frac{R_1}{R_2}\frac{V_s}{V_{\text{in}}} \quad \Rightarrow \quad T_2 = R_2\,C\,\ln\left(1 + \frac{R_1}{R_2}\,\frac{V_s}{V_{\text{in}}}\right) \approx R_1 C \frac{V_s}{V_{\text{in}}}.$$

Thus, the square wave oscillation is cyclically "on" ($V_{\text{out}} = V_s$) for a period T_1 and then "off" ($V_{\text{out}} = 0$) for a period T_2, with duty cycle D and frequency ω given by

$$D \triangleq \frac{T_1}{T_1 + T_2} \approx \frac{V_{\text{in}}}{V_s}, \quad \omega = \frac{1}{T_1 + T_2} \approx \frac{V_{\text{in}}(V_s - V_{\text{in}})}{R_1\,C\,V_s^2}\ \text{Hz}.$$

Unfortunately, the frequency of the simple oscillator described above varies with V_{in}, with $\omega \to 0$ as $V_{\text{in}}/V_s \to 0$ and as $V_{\text{in}}/V_s \to 1$. A significantly improved PWM circuit, which operates at a constant (independent of V_{in}) frequency $\omega = 1/(4\,R_3\,C)$ Hz, is given by cascading together the three stages shown in Figure 10.29. The first stage (Figure 10.29a) is a passive voltage divider with $V_o = V_s/2$, with a capacitor added to stabilize the output voltage in case the (small) load attached to its output fluctuates; values of $R \sim 10\,\text{k}\Omega$ and $C \sim 100$ nF are typical. The second stage (Figure 10.29b) generates a triangle wave V_w between 0 and V_s and operating at a frequency of $\omega = 1/(4\,R_1\,C)$ Hz, as discussed below. Finally, the third stage (Figure 10.29c) compares the triangle wave V_w with V_{in}, outputting V_s whenever V_{in} is greater than V_w, and outputting 0 whenever V_{in} is less than V_w, thus resulting in a duty cycle of V_{in}/V_s.

To analyze the operation of the triangle-wave generator of Figure 10.29b, denote the inputs and outputs of op amp A (configured in an unstable configuration with positive feedback) as $\{V_{\text{A},+}, V_{\text{A},-} = V_o, V_{\text{A,out}}\}$, and denote the inputs and outputs of op amp B (configured in a stable configuration with negative feedback) as $\{V_{\text{B},+} = V_o, V_{\text{B},-}, V_{\text{B,out}} = V_w\}$. Note that, since op amp B is wired with (stabilizing) negative feedback, $V_{\text{B,out}}$

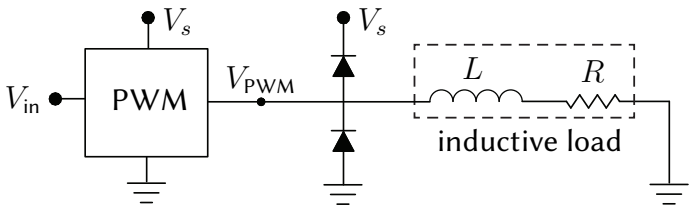


Figure 10.30: Application of a PWM circuit, formed by cascading the three stages of Figure 10.29, to an inductive load, incorporating a pair of protective **flyback diodes** to prevent voltage spikes from forming at V_{PWM} (and, possibly, an arc between exposed wires, and/or damage to one of the op amps) when the PWM circuit acts to quickly turn the power on and off to an inductive load.

adjusts so that $V_{\text{B},-} = V_{\text{B},+} = V_o = V_s/2$ at all times. Note also that resistors R_2 and R_3 form another voltage divider so that, taking[34] $R_2 \approx R_3$, it follows that $V_{\text{A},+} = (V_{\text{A,out}} + V_{\text{B,out}})/2$ at all times. As in the oscillator circuits considered previously, there are two states to consider:

(a) $V_{\text{A,out}} = 0$. Assuming the capacitor is initially charged such that $V_{\text{B,out}} = 0$, current flows from the output of op amp B through C and R_1 to the output of op amp A, charging the capacitor until $V_{\text{B,out}} = V_s$ and thus $V_{\text{A},+}$ just[34] exceeds $V_{\text{A},-} = V_s/2$, and op amp A flips to state (b).

(b) $V_{\text{A,out}} = V_s$. Assuming the capacitor is initially charged such that $V_{\text{B,out}} = V_s$, current flows from the output of op amp A through R_1 and C to the output of op amp B, charging the capacitor until $V_{\text{B,out}} = 0$ and thus $V_{\text{A},+}$ falls just[34] below $V_{\text{A},-} = V_s/2$, and op amp A flips back to state (a).

The period of this oscillation is constant, and may be calculated by determining how long it takes the capacitor of the relaxation oscillator to gather sufficient charge to flip the switch in each state. For example, taking $V_{\text{A,out}} = 0$ and $V_{\text{B,out}}(0) = 0$, the dynamics of state (a) are governed by

$$C\frac{d}{dt}(V_{\text{B,out}} - V_{\text{B},-}) = \frac{V_{\text{B},-} - V_{\text{A,out}}}{R_1} \quad \Rightarrow \quad R_1\,C\,\frac{d}{dt}V_{\text{B,out}} = V_{\text{B},-} - V_{\text{A,out}} \quad \Rightarrow$$
$$V_{\text{B,out}}(t) = \frac{1}{R_1\,C}(V_{\text{B},-} - V_{\text{A,out}})t, \quad V_{\text{B,out}}(T/2) = V_s \quad \Rightarrow \quad T = 4\,R_1\,C.$$

Example 10.30 Efficient power control of inductive loads via pulse width modulation. The PWM strategy for driving loads at partial power, as described above, is highly efficient and remarkably inexpensive to implement with modern electronics. If applied to a load with inductance, however, a problem is encountered. The PWM effectively acts as a switch, quickly turning on and off the power to (and, thus, the current through) the attached load. If the load contains an inductor governed by $V = L\ dI/dt$ [see (10.2c)], rapid changes in the current through the inductor would tend to induce large voltage spikes at V_{PWM}. As introduced in Figure 10.18, the diodes used in the circuit in Figure 10.30, called **flyback** (a.k.a. **snubber**, **freewheeling**, or **suppressor**) diodes, ensure (by providing a current path from ground, or to power, when necessary) that V_{PWM} does not exceed the range $-V_{\text{d}}$ to $V_s + V_d$, where V_{d} is the (small) cut-in voltage of the diode. *A good PWM circuit should always have such a flyback diodes incorporated, just in case the load attached to the PWM circuit has inductive elements.*

[34] Note that R_3 should actually be chosen to be just slightly smaller than R_2, so that $V_{\text{A},+} = (0.5 - \epsilon)V_{\text{A,out}} + (0.5 + \epsilon)V_{\text{B,out}}$, and the states indeed flip as described. This can be achieved by selecting two resistors of the same rated resistance and, say, 5% variance, then carefully measuring the resistance of the two and and putting the one with smaller resistance in the R_3 location.

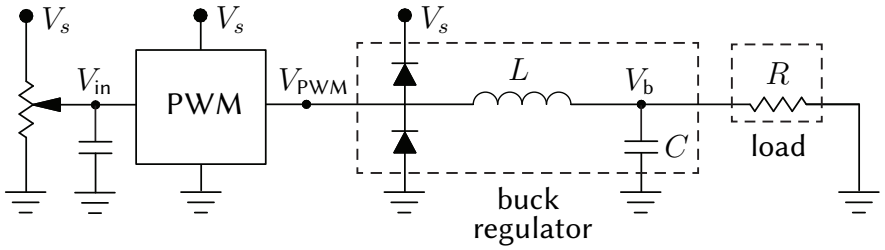


Figure 10.31: Application of a **buck regulator** for DC/DC conversion. A variable voltage divider (stabilized by a capacitor) may be used to generate an input V_{in} to a PWM circuit, such as that given by cascading the stages shown in Figure 10.29. The output of the PWM is then buffered with an inductor, capacitor, and a pair of flyback diodes, that together act as a **second-order low-pass filter** (see Example 10.2) which passively and efficiently removes the square wave from the PWM signal *without the losses associated with extra resistive elements*.

Figure 10.32: The (left) external wiring and (right) internal circuitry of the TI TPS56637.

Example 10.31 Buck converters. The circuit developed in Example 10.30 is one step away from that illustrated in Figure 10.31, called a **buck converter**, which efficiently solves the problem of DC-DC voltage step-down common in computers and electromechanical systems [cf. the **boost converter** discussed in Example 10.20]. Assuming a square wave at V_{PWM}, with current flowing from the PWM circuit when $V_{\text{PWM}} = V_s$ and current flowing from ground (through the diode) when $V_{\text{PWM}} \approx 0$, and assuming (for the purpose of analysis) that the load is essentially resistive with some resistance R, V_{b} is determined as follows:

$$V_{\text{PWM}} - V_{\text{b}} = L\,\frac{dI_L}{dt}, \quad C\,\frac{dV_{\text{b}}}{dt} = I_C, \quad V_{\text{b}} = I_R\,R, \quad I_L = I_C + I_R \quad \Rightarrow \quad \frac{V_{\text{b}}(s)}{V_{\text{PWM}}(s)} = \frac{1/(L\,C)}{s^2 + s/(R\,C) + 1/(L\,C)}.$$

Thus, regardless of the precise value of R, if L and C are selected to be large enough that $\omega^2 \gg 1/(L\,C)$, where ω is the frequency of square wave output by the PWM, then the fundamental and higher harmonics of the square wave will be damped by the second-order low-pass filter in the buck converter, leaving only the average value of the PWM signal, which as derived previously is simply V_{in}, which is set by the user. Note also that, if a precise value is required for V_{in}, an appropriately-selected Zener diode may be used instead of the lower half of the resistor in the first stage of the circuit illustrated in Figure 10.31.

Implementation. As in the boost converter case of Example 10.20, rather than running at a fixed duty cycle, *feedback* can again be implemented to identify the duty cycle D required to more precisely achieve a desired value of $V_b = V_{\text{PWM}}^{\text{mean}}$. This may be achieved, e.g., by implementing a TI TPS56637, which is compact (less than 9 mm^2), easy to hook up (SMT, 5 pins), and inexpensive ($0.27). The (simple) external wiring and (complicated) internal circuitry diagrams for the LMR62014 (which generates the required PWM signal with a few op amps) are illustrated in Figure 10.32; note that $\{L, d, C\}$ on the previous page correspond to $\{L1, D1, C2\}$ in the external wiring diagram, and the button b is replaced by a PWM-actuated MOSFET illustrated near the right side of the internal circuitry diagram. $V_{\text{out}}(t)$ may then be hooked to a load of a few hundred ohms, and this circuit will drive the tens of mA necessary to drive this load. Note also that the $I_L(t)$ plot given in Figure 10.22 also appears on page 12 of the LMR62014 datasheet.

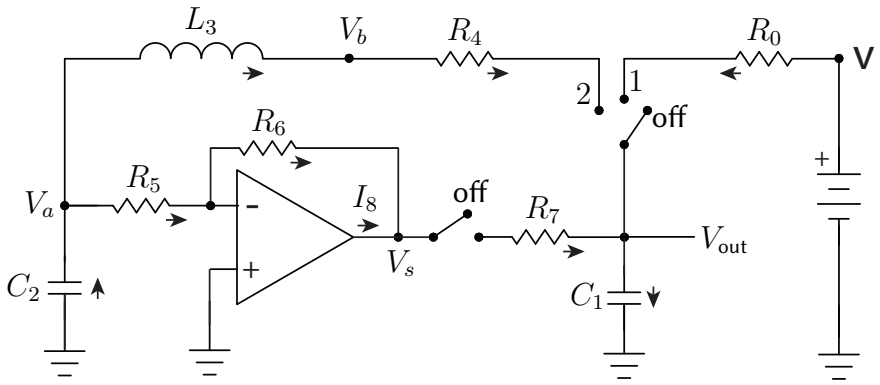


Figure 10.33: The **Colpitts oscillator** considered in Example 10.32.

Example 10.32 Colpitts oscillator. A Colpitts oscillator is an LC tank oscillator (see Example 10.11) with a simple transistor or op amp circuit implemented in order to offset the losses associated with the inevitable resistance of the real components in the circuit, thereby exhibiting sustained oscillations. We will consider here the case with an op amp implemented, as illustrated in Figure 10.33 (cf. Figure 10.11), initialized with both switches in the **off** position, current equal to zero everywhere, and all capacitors fully discharged.

Startup. Startup of the Colpitts oscillator, which occurs when we turn the switch from off to **position 1** (leaving the 2-way switch at **off**), is the same as the startup of the LC tank oscillator discussed in Example 10.11.

Decaying oscillations. Starting from the steady values of $V_{\text{out}}(t) = V_s$ and $I_1(t) = 0$, moving the 3-way switch from position 1 to **position 2** (leaving the 2-way switch at **off**) initiates sinusoidal oscillations that gradually decay due to the inevitable parasitic resistance of the components in the circuit. Analysis of these oscillations is the same as the analysis of the decaying oscillations of the LC tank oscillator discussed in Example 10.11.

Sustained oscillations. Some time after starting the oscillations discussed above, we turn the 2-way switch from off to **on** (leaving the 3-way switch at **position 2**), thereby attaching the op amp to the LC tank oscillator. Selecting $\{R_5, R_6, R_7\}$ appropriately, the net effect of hooking in this op amp is to provide just enough energy back into the oscillations, phased appropriately, to make up for the energy lost in R_4.

To derive the equations governing this circuit, we extend the analysis of the LC tank in Example 10.11, modifying the statements of KCL as appropriate (include I_8, the current coming out of the op amp), incorporating the component equations for $\{R_5, R_6, R_7\}$, and applying the relation $V_- = V_+ = 0$ to account for the behavior of the op amp, which is implemented in the stable (negative feedback) configuration. We assume that, when the 2-way switch is turned on [taken here as $t = 0$], $V_{\text{out}}(t=0) = V_{\text{out}}^0$, $V_a(t=0) = V_a^0$, and $I_3 = I_3^0$. The Laplace transforms of $\{V'_{\text{out}}(t), V'_a(t), I'_3(t)\}$ are thus $(s\,V_{\text{out}}(s) - V_{\text{out}}^0)$, $(s\,V_a(s) - V_a^0)$, and $(s\,I_3(s) - I_3^0)$, and our 12 governing eqns (5 KCLs and 7 components) are:

$$I_2(s) = I_3(s) + I_5(s), \quad I_3(s) = I_4(s), \quad I_4(s) + I_7(s) = I_1(s), \quad I_5(s) = I_6(s), \quad I_6(s) + I_8(s) = I_7(s),$$
$$I_1(s) = C_1[s\,V_{\text{out}}(s) - V_{\text{out}}^0], \quad I_2(s) = -C_2\,[s\,V_a(s) - V_a^0], \quad V_a(s) - V_b(s) = L_3\,[s\,I_3(s) - I_3^0],$$
$$V_b(s) - V_{\text{out}}(s) = R_4\,I_4(s), \quad V_a(s) = R_5\,I_5(s), \quad -V_s(s) = R_6\,I_6(s), \quad V_s - V_{\text{out}}(s) = R_7\,I_7.$$

Thus, 12 linear eqns in 12 variables $\{I_1(s), I_2(s), I_3(s), I_4(s), I_5(s), I_6(s), I_7(s), V_a(s), V_b(s), V_{\text{out}}(s)\}$, the first 11 of which are to be eliminated, as easily solved via Matlab (see code in RR Chapter 10), thus giving:

$$V_{\text{out}}(s) = \frac{b_2 s^2 + b_1 s + b_0}{s^3 + a_2 s^2 + a_1 s + a_0} = \frac{b_2 s^2 + b_1 s + b_0}{(s + a_3)[s^2 + a_4 s + a_5]} \quad \text{where} \tag{10.23}$$

$$a_2 = \frac{C_1\,C_2\,R_4\,R_5\,R_7 + C_2\,L_3\,R_5 + C_1\,L_3\,R_7}{C_1\,C_2\,L_3\,R_5\,R_7}, \quad a_1 = \frac{L_3 + C_2\,R_4\,R_5 + C_1\,R_4\,R_7 + C_1\,R_5\,R_7 + C_2\,R_5\,R_7}{C_1\,C_2\,L_3\,R_5\,R_7}, \quad a_0 = \frac{R_4 + R_5 + R_6 + R_7}{C_1\,C_2\,L_3\,R_5\,R_7}.$$

The values of $\{a_2, a_1, a_0\}$, all of which are seen to be positive, determine the behavior of the solution. The values of $\{b_2, b_1, b_0\}$ just determine the coefficients of the solution components that are present, based on the precise values of $\{V_{\text{out}}^0, V_a^0, I_3^0\}$, and are not considered further here.

Factoring the denominator of (10.23), a_3 may be determined via Cardano's formula: taking $q = (3\,a_1 - a_2^2)/3$, $r = (2\,a_2^3 - 9\,a_2\,a_1 + 27\,a_0)/27$, and $d = r^2/4 + q^3/27$, it follows that $a_3 = a_2/3 - \sqrt[3]{-r/2 + \sqrt{d}} - \sqrt[3]{-r/2 - \sqrt{d}}$, where $\sqrt[3]{x}$ denotes the principal (that is, the real) 3rd root of the real number x. It then follows immediately that $a_4 = a_2 - a_3$ and $a_5 = a_0/a_3$. The variables $\{a_3, a_4, a_5\}$ are determined from $\{C_1, C_2, L_3, R_4, R_5, R_6, R_7\}$ by the Barkhausen condition code in RR Chapter 10. It turns out that $a_3 > 0$ and $a_5 > 0$ [that is, the first term in the denominator of $V_{\text{out}}(s)$ is stable, and the second term is oscillatory] if all seven of these parameters are positive. The oscillatory term has:

- *positive* damping (thus, damped oscillations) if $a_4 > 0$, and
- *negative* damping (thus, sustained oscillations) if $a_4 < 0$ (this is known as the **Barkhausen criterion**).

If $a_4 < 0$, the oscillations grow until the output of the op amp reaches the minimum and maximum values of the power supply itself, after which the clipping of the op amp output [see (10.19)] reduces its effective gain slightly, and a periodic, essentially sinusoidal oscillation is established.

When designing a Colpitts oscillator of the form illustrated in Figure 10.33, one first selects $\{C_1, C_2, L_3\}$ such that the LC tank part of the circuit (see Example 10.11) oscillates at the desired frequency, $\omega_d = 1/\sqrt{L_3 C}$ where $1/C = 1/C_1 + 1/C_2$. Often a balanced configuration is chosen, with $C_1 = C_2$. In this design, a tradeoff is made, keeping both the capacitors and the inductor sufficiently small to minimize the overall size, cost, and parasitic resistance (modeled as R_4 in this analysis) of the components selected. Intermediate values of R_5 and R_7 are then assigned, to keep the current demands on the op amp relatively small. Finally, one then tunes R_6 in order to make a_4 slightly negative, thus sustaining the oscillations; for example, taking $C_1 = C_2 = 1\,\mu\text{F}$, $L_3 = 1\,\text{mH}$, $R_4 = 1\,\Omega$, $R_5 = 1\,\text{k}\Omega$, and $R_7 = 100\,\Omega$, it is found that $R_6 \approx 1325\,\Omega$ achieves this goal. Large negative values of Ω are not desired, as they put proportionally more work on the op amp (which costs power) and less on the passive components of the LC tank.

Note that, if R_7 is taken as zero, it is not possible to satisfy the Barkhausen criterion, and thus sustain oscillations with an op-amp reinforced Colpitts oscillator circuit. This is despite several (explicit or implied) false claims to the contrary online (as of 2021, do a Google image search yourself), and even a couple of well-meaning textbooks; Jakas & Llopis (2007) discuss this confusion in detail.

10.4 Signal transmission

This chapter still under construction.

10.4.1 Digital logic and storage elements

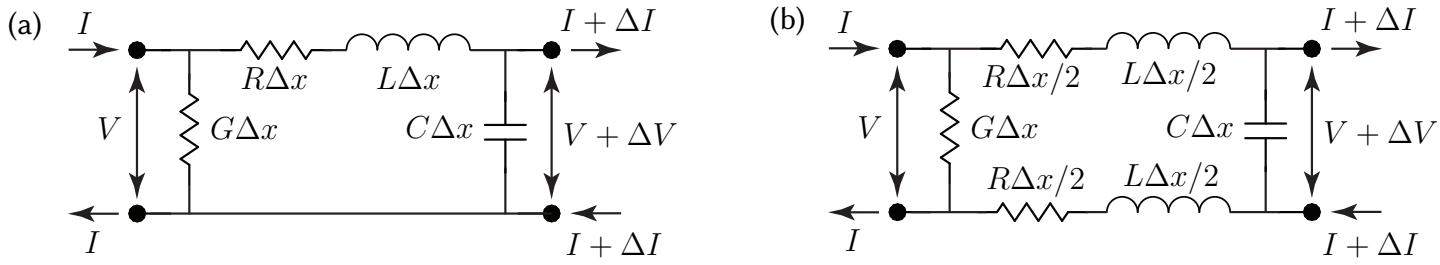


Figure 10.34: Two equivalent models of a section, of length Δx, of a pair of transmission wires.

10.4.2 Telegrapher's equation and characteristic impedance

Consider the models for the electrical characteristics of a pair of transmission wires illustrated in Figure 10.34. Note that, in this section (§10.4.2) only, we follow the dominant convention in the literature, and indicate by $\{R, L, G, C\}$ the resistance *per unit length*[35] (along the pair of wires), the inductance *per unit length* (along the pair of wires), the conductance[36] *per unit length* (between the two wires), and the capacitance *per unit length* (between the two wires). These quantities might more precisely be denoted as $\{dR/dx, dL/dx, dG/dx, dC/dx\}$, respectively, but that would be notationally too heavy in the derivation that follows.

The equations that govern the electrical signals that propagate down the pair of wires in this model (either Figure 10.34a or, equivalently, Figure 10.34b) may be written simply by expressing, over a short length of wire Δx, the change in voltage between the two wires, ΔV, and the change in current flowing within the wires, ΔI, using the basic "lumped parameter" component equations (10.2a)-(10.2c), which easily gives

$$\Delta V = -(R\,\Delta x)I - (L\,\Delta x)\frac{dI}{dt}, \qquad \Delta I = -(G\,\Delta x)V - (C\,\Delta x)\frac{dV}{dt}. \tag{10.24a}$$

Dividing both equations by Δx, then taking the limit as $\Delta x \to 0$, thus gives the telgrapher's equations

$$\frac{dV}{dx} = -\Big(R + L\frac{d}{dt}\Big)I, \qquad \frac{dI}{dx} = -\Big(G + C\frac{d}{dt}\Big)V. \tag{10.24b}$$

Taking d/dx of the first equation and inserting the second gives a scalar second-order form of this PDE,

$$\frac{d^2V}{dx^2} = \Big(R + L\frac{d}{dt}\Big)\Big(G + C\frac{d}{dt}\Big)V. \tag{10.25}$$

Following a **separation of variables** (SOV) solution approach, we seek solution modes of the **separable** form

$$V^m(x,t) = X^m(x)\,T^m(t). \tag{10.26}$$

Inserting the assumed form of the solution (10.26), aka the **solution ansatz**, into the PDE (10.25), and isolating the spatial dependence on one side of the equation and the time dependence on the other side, gives

$$X''\,T = R\,G\,X\,T + (R\,C + L\,G)X\,T' + L\,C\,X\,T'' \quad \Rightarrow \quad \frac{X''}{X} = \frac{R\,G\,T + (R\,C + L\,G)T' + L\,C\,T''}{T} = -k^2,$$

[35] The resistance per unit length of a wire (measured in ohms per meter, Ω/m) can be found by dividing the **resistivity** ρ of its conductive material (measured in ohm meters, Ω m) by its cross-sectional (measured in square meters, m^2).

[36] Conductance is simply the reciprocal of the resistance, and is sometimes a useful characteristic to use in settings (like, between to wires in a transmission line system) where the resistance between two points is either very large or essentially infinite. The **siemens** (**S**) is the unit of electric conductance in SI; a siemens (also referred to as a mho) is thus equal to the reciprocal of an ohm, $S = 1/\Omega$.

where k is a constant (that is, neither a function of x, nor a function of t). Note that we have dropped the $()^m$ superscripts, and the (x) and (t) dependencies, for notational clarity. We thus have

$$X'' + k^2 X = 0 \quad \Rightarrow \quad X(x) = X_+ e^{\mathrm{i}kx} + X_- e^{-\mathrm{i}kx}, \tag{10.27a}$$

$$a\,T'' + b\,T' + c\,T = 0 \quad \Rightarrow \quad T(t) = T_+ e^{\mathrm{i}\omega_+ t} + T_- e^{\mathrm{i}\omega_- x}, \tag{10.27b}$$

where $a = L\,C$, $b = R\,C + L\,G$, $c = R\,G + k^2$, and $-a\,\omega^2 + \mathrm{i}\,b\,\omega + c = 0$, and thus

$$L\,C\,\omega^2 - \mathrm{i}\,(R\,C + L\,G)\,\omega - R\,G = k^2 = \omega^2\,L\,C\Big(1 - \frac{\mathrm{i}\,(R\,C + L\,G)}{\omega\,L\,C} + \frac{\mathrm{i}^2 R\,G}{\omega^2\,L\,C}\Big),$$

and therefore

$$k = \omega\,\sqrt{L\,C}\,\sqrt{\Big(1 - \frac{\mathrm{i}\,R}{\omega\,L}\Big)\Big(1 - \frac{\mathrm{i}\,G}{\omega\,C}\Big)} \quad \Leftrightarrow \quad \mathrm{i}\,k = \sqrt{(\mathrm{i}\,\omega\,L + R)(\mathrm{i}\,\omega\,C + G)}; \tag{10.28}$$

this is known as a **dispersion relation** of the transmission line system. Note that,

$$\text{if } \frac{R}{\omega\,L} \ll 1 \text{ and } \frac{G}{\omega\,C} \ll 1, \text{ it follows that } k \approx \omega\,\sqrt{L\,C}; \tag{10.29}$$

this common case, with low resistance per unit length, R, along the wire, and low conductance (the inverse of resistance) per unit length, G, from one wire to the other, corresponds to modes [see (10.26) and (10.27)] of the general form $V^m(x,t) = A e^{\mathrm{i}(kx+\omega t)} = A e^{\mathrm{i}k(x+ct)}$, where the wave speed $c = \omega/k = 1/\sqrt{L\,C}$ is real (and, less than the speed of light, which is the speed that electrons themselves move). In other words, this case is characterized by waves that propagate without distortion in shape[37]. If one or both of the terms at left in (10.29) is not small, then the dispersion relation is not a simple real, linear relationship between k and ω, and the wave suffers some distortion (in shape) and attenuation (reduction in magnitude) as it travels down the wire.

We now put the voltage and corresponding current components of the solution back together. By (10.26), (10.27), and (10.24b), one component of the voltage and current modal solutions [other modal components can be written with different signs on k and ω] may be written

$$V^m(x,t) = V_o\,e^{\mathrm{i}kx} e^{\mathrm{i}\omega t}, \quad I^m(x,t) = -I_o\,e^{\mathrm{i}kx} e^{\mathrm{i}\omega t}, \tag{10.30}$$

where, by both equations given in (10.24b) and the expression at right in (10.28), we may write

$$\left.\begin{aligned} \mathrm{i}\,k\,V_o = (\mathrm{i}\,\omega\,L + R) I_o \quad &\Rightarrow \quad \frac{V_o}{I_o} = \frac{(\mathrm{i}\,\omega\,L + R)}{\mathrm{i}\,k} \\ \mathrm{i}\,k\,I_o = (\mathrm{i}\,\omega\,C + G) V_o \quad &\Rightarrow \quad \frac{V_o}{I_o} = \frac{\mathrm{i}\,k}{(\mathrm{i}\,\omega\,C + G)} \end{aligned}\right\} \quad \Rightarrow \quad \frac{V_o}{I_o} = \sqrt{\frac{\mathrm{i}\,\omega\,L + R}{\mathrm{i}\,\omega\,C + G}} = Z_o; \tag{10.31}$$

note that the **characteristic impedance** of the system, Z_o, is measured in ohms. Note also that,

$$\text{if } \frac{R}{\omega\,L} \ll 1 \text{ and } \frac{G}{\omega\,C} \ll 1, \text{ it follows that } Z_o = \frac{V_o}{I_o} \approx \sqrt{\frac{L}{C}}. \tag{10.32}$$

Again, this case, with low resistance per unit length, R, along the wires, and low conductance (the inverse of resistance) per unit length, G, from one wire to the other, is quite common. Note that, in this case, the characteristic impedance Z_o (measured in ohms) arises primarily due to the L and C terms in the model [see (10.24)] of the transmission line system.

Typical values (for Cat 5e ethernet cable; other cables are similar) are $L = 525$ nH/m and $C = 52$ pF/m, and thus $Z_o = \sqrt{L/C} = \sqrt{(525 \cdot 10^{-9})/(52 \cdot 10^{-12})} = 100$ ohm and $c = 1/\sqrt{L\,C} = 1.9 \cdot 10^8$ m/s. Note that this wave propagation speed c is about 2/3 of the speed of light in a vacuum, which is $2.99792 \cdot 10^8$ m/s.

[37] How much of each mode is present in the overall solution, which may be formed as a superposition of modes of the form given in (10.26), is a function of the boundary conditions and initial conditions on the system, which we do not explore further here.

Example 10.33 Termination, impedance matching, and signal distortion. Consider the transmission line model illustrated in Figure 10.34a, with the voltage of the lower wire defined as ground, and with a specified $\{R, L, G, C\}$ (see §10.4.2). We now model the voltage $V(x,t)$ and current $I(x,t)$ propagating along the upper wire by discretizing the linear PDE (10.24b), rearranged into the form

$$\frac{d}{dt}\begin{pmatrix} V \\ I \end{pmatrix} = -\begin{pmatrix} G/C & (1/C)\,d/dx \\ (1/L)\,d/dx & R/L \end{pmatrix}\begin{pmatrix} V \\ I \end{pmatrix}, \tag{10.33}$$

starting from the initial condition that the wire starts out with zero voltage and zero current everywhere, that is, $V(x, t=0) = I(x, t=0) = 0$. We will apply a boundary condition on the voltage at the left end of the wire, $V(x=0,t)$, that transitions fairly smoothly from $V=0$ to $V=2$ after $t=0$, according to

$$V(x=0,t) = \begin{cases} 1-\cos(\pi t/t_1) & 0 \le t \le t_1, \\ 2 & t_1 \le t, \end{cases} \tag{10.34}$$

where $t_1 = 10^{-8}$ s. We will initially, in Case A below, consider a simple case with a zero boundary condition on the current at the right end of the wire, $I(x=X,t)$. [We will change this in Example 10.33.]

We first prepare to numerically simulate both wave components, $V(x,t)$ and $I(x,t)$, as they propagate down the transmission line for $0 < x < X$ and $t > 0$. We do this by discretizing the PDE + BCs with simple numerical methods (see §10), as described below, using sufficiently small grid spacing in time and space (that is, small Δt and Δx) in the numerical discretization such that reducing Δt and Δx further does not substantially change the numerical result. Other numerical methods would certainly be more efficient and better behaved for larger Δx and Δt, but the simple approach implemented here proves to be adequate.

We start by discretizing $V(x,t)$ on a spatial grid with $x_i = i\Delta x$, denoting $V_i(t) = V(x_i,t)$. Noting that (10.33) is characterized by *first-order derivatives* in space, we discretize I on a grid that is *staggered* with respect to the grid used to discretize V, denoting $I_{i+0.5}(t) = I(x_{i+0.5},t)$ where $x_{i+0.5} = (i+0.5)\Delta x$ for integer i.

The grid is defined by taking $\Delta x = X/(N+0.5)$, so the rightmost gridpoint, at $x=X$, is the gridpoint corresponding to $I_{N+1/2}(t)$; this will make implementing the BC $I(x=X,t)$ particularly easy. Note that, using this grid, there are N integer gridpoints on the interior, at which $V_1(t)$ to $V_N(t)$ are defined, and there are N fractional gridpoints on the interior, at which $I_{0.5}(t)$ to $I_{N-0.5}(t)$ are defined.

We apply the BC on $V_0(t)$ as a forcing term on the RHS, and note that the BC $I(x=X,t)=0$ may be enforced simply by dropping this term from the discretized equations. We discretize the PDE in (10.33) with second-order central discretizations of the dI/dx and dV/dx terms; the staggered grid implemented makes this approach work particularly well. Defining $d = 1/\Delta x$, this is accomplished with a linear system of the general form

$$d\mathbf{x}/dt = A\mathbf{x} + BV_0(t) \tag{10.35}$$

$$\mathbf{x}(t) = \begin{pmatrix} I_{0.5}(t) \\ V_1(t) \\ I_{1.5}(t) \\ V_2(t) \\ \vdots \\ I_{N-0.5}(t) \\ V_N(t) \end{pmatrix}, \quad A = \begin{pmatrix} -R/L & -d/L & & & & & & 0 \\ d/C & -G/C & -d/C & & & & & \\ & d/L & -R/L & -d/L & & & & \\ & & d/C & -G/C & -d/C & & & \\ & & & \ddots & \ddots & \ddots & & \\ & & & & d/L & -R/L & -d/L & \\ & & & & & d/C & -G/C & \\ 0 & & & & & & & \end{pmatrix}, \quad B = \begin{pmatrix} d/L \\ 0 \\ 0 \\ 0 \\ \vdots \\ 0 \\ 0 \end{pmatrix}.$$

Denoting $h = \Delta t$, $t_n = hn$, $\mathbf{x}_n = \mathbf{x}(t_n)$, and $V_{0,n} = V_0(t_n)$, a CN method is used to propagate (10.35):

$$\frac{\mathbf{x}_n - \mathbf{x}_{n-1}}{h} = \frac{A}{2}\Big[\mathbf{x}_n + \mathbf{x}_{n-1}\Big] + B\,V_{0,n-0.5} \quad \Rightarrow \quad \Big[I - \frac{A\,h}{2}\Big]\mathbf{x}_n = \Big[I + \frac{A\,h}{2}\Big]\mathbf{x}_{n-1} + B\,h\,V_{0,n-0.5} = \mathbf{r}_{n-0.5}.$$

The system $[I - A\,h/2]\,\mathbf{x}_n = \mathbf{r}_{n-0.5}$ may be solved efficiently at each timestep using a reduced form of Gaussian elimination that accounts for the fact that A is tridiagonal and, for sufficiently small h, diagonally dominant. A simple code that performs the simulation described above, but quite *inefficiently* (but, good enough for the present purposes, if you have a fast computer, and choose the number of gridpoints used, N, to be sufficiently small), is given in Algorithm **??**; this code simply calculates `x=D\r` at each timestep, where $D = I - A\,h/2$ and $\mathbf{r} = [I + A\,h/2]\mathbf{x} + B\,hV_{0,n-0.5}$. Egregiously, the code stores D as a full matrix, which indeed is *not at all* efficient. The implementation of a *computationally efficient* numerical method for this simulation, leveraging the Thomas algorithm, is discussed in Example **??**.

The simulations listed below take parameter values typical values for Cat 5e ethernet cable ($R = G \approx 0$, $L = 525 \cdot 10^{-9}$ H/m, and $C = 52 \cdot 10^{-12}$ F/m, and thus $c = 1.9 \cdot 10^8$ m/s and $Z_0 = 100\,\Omega$; see the last paragraph of §10.4.2). We will consider a wire length of $X = 10$ m, and thus expect the wave traveling along the wire to begin to reach the rightmost boundary at $T = X/c = 5.22 \cdot 10^{-8}$ s. We will use a timestep of $h = \Delta t = 4 \cdot 10^{-11}$ s, and a spatial grid spacing with $N = 200$, and thus $\Delta x = X/(N + 0.5) = 0.049875$ m.

Case A: No termination. In this case, the boundary condition at the right edge of the domain is taken as $I(x = L, t) = I_{N+1/2}(t) = 0$ [that is, no significant current into the downstream component, which accurately models a connection to the input of an op amp]. In the representation (10.35), this term is simply set to zero, so the last component of the $\mathbf{x}$ vector is $V_N(t)$, and the dependence of the evolution equation on $I_{N+1/2}(t)$ is simply dropped.

The resulting wave propagation is illustrated in Figure 10.35. Note that the wave is reflected back and forth across the domain indefinitely, causing spurious echos in the communication channel (akin to talking over a phone line or PA system in the presence of undamped feedback).

Case B: Termination with a resistor. In this example, the boundary conditions at the right edge of the domain is changed to model the effect of a single resistor, with resistance Z_0, installed between the two wires at $x = X$. We do this by taking $I_{N+1/2}(t) = (1/Z_0)V_N(t)$.

Again taking $R = G = 0$, $L = 525 \cdot 10^{-9}$, and $C = 52 \cdot 10^{-12}$, the resulting wave propagation is illustrated in Figure 10.36. Note that the wave reflections have been eliminated. Problem solved.

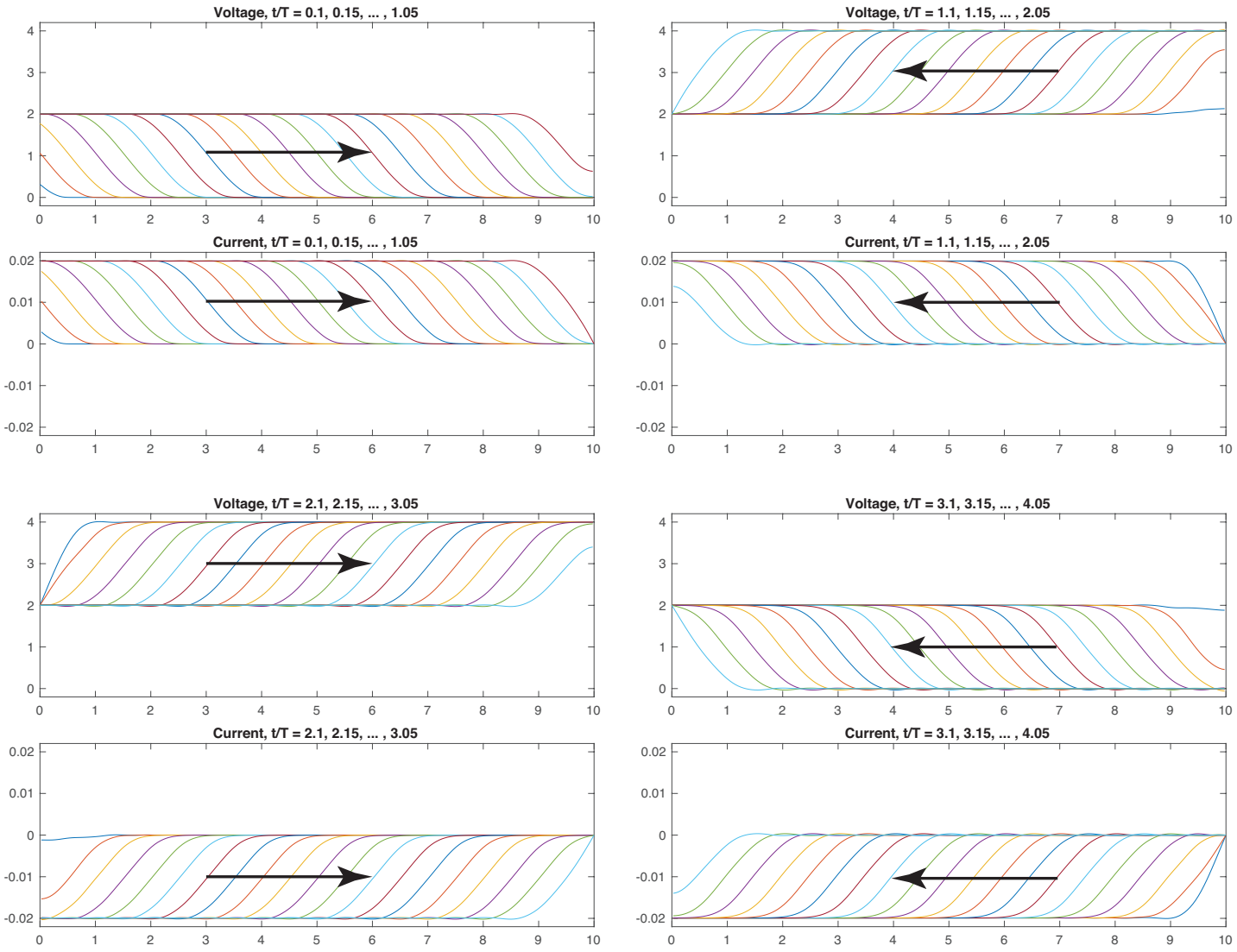


Figure 10.35: Transmission of a signal down a wire as in Case A of Example 10.33, with **no termination**. Note that, if $R = G = 0$, the signal reflects back and forth over the wire indefinitely.

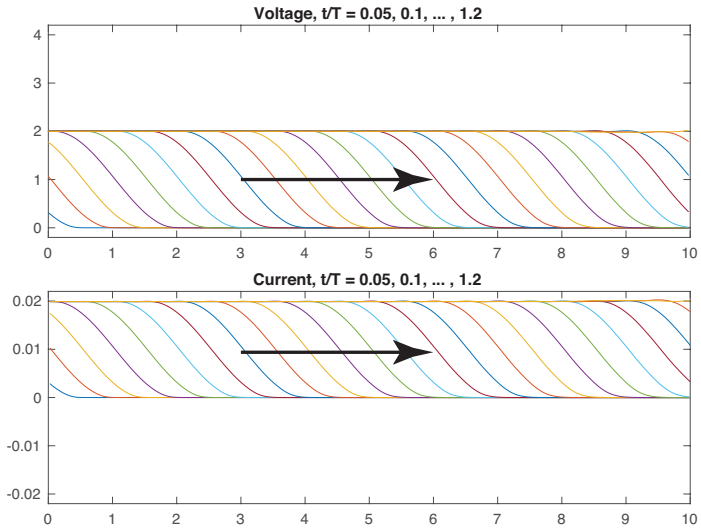


Figure 10.36: Transmission of a signal as in Example 10.33, implementing a **terminating** resistor of Z_0 ohms. The signal reflection is eliminated; after $t/T = 1.2$, $V(x,t) \approx 2$ and $I(x,t) \approx 0.02$ along the entire wire.

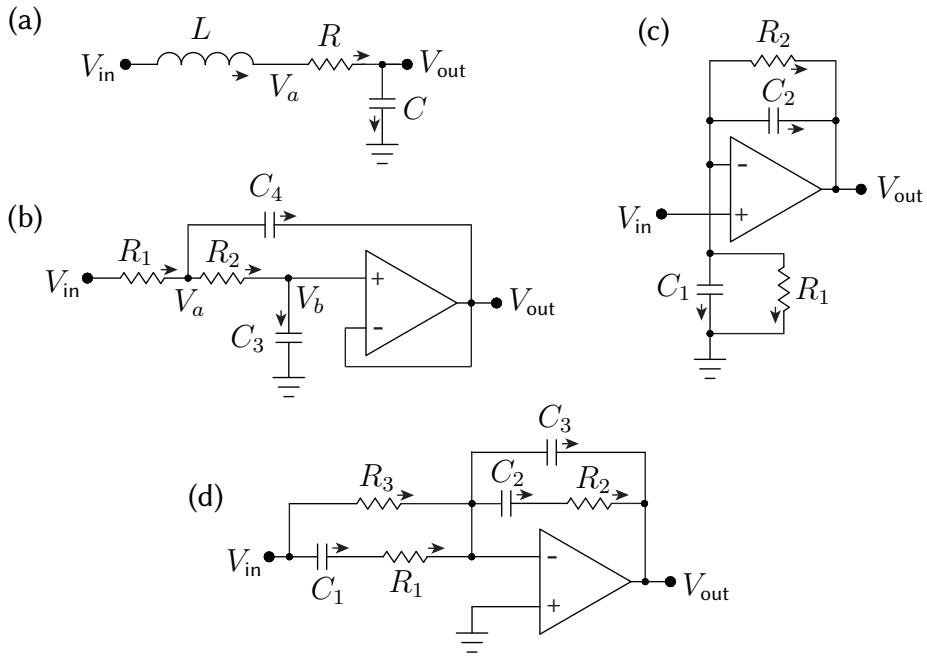


Figure 10.37: Some dynamic filters considered in the exercises. (a) A passive second-order low-pass filter. (b) An active second-order low-pass filter. (c) A general-purpose noninverting first-order filter. (d) A single op-amp implementation of a PID filter combined with two first-order low-pass filters.

Example 10.34 Wire junction. In the...

Exercises

[*Note: Put all numerical codes you write to solve these exercises, with appropriate (succinct, clear) comments to make them readable, in a private repository in your account on Github, share this repository with the course instructors, and provide links to these codes in the pdfs of your homework writeups that you submit for the class.*]

Exercise 10.1 Following an analogous derivation as that in Example 10.4, replace the six resistors in Figure 10.5a-b with six capacitors $\{C_1, C_2, C_3, C_a, C_b, C_c\}$, and write a code `Wye_Delta_Capacitors.m` that quantifies $\{C_a, C_b, C_c\}$ in terms of $\{C_1, C_2, C_3\}$, and vice versa, so that the two circuits are equivalent. Then, replacing the five resistors in Figure 10.4d with five capacitors $\{C_1, C_2, C_3, C_4, C_5\}$ and applying this result, compute the equivalent capacitance C of this network. *Note: Given the simple path to solution in this problem using symbolic manipulation, the engineering student is encouraged to to crank through such tedious algebraic manipulations symbolically whenever possible from now on!*

Exercise 10.2 Following an analogous derivation as that in Example 10.5, given one inductor L_2 of a precisely known inductance, write a code `Wheatstone_Inductors.m` that quantifies how a Wheatstone bridge may be used to measure the inductance of an unknown inductor L_5.

Exercise 10.3 Following an analogous derivation as that in Example 10.7, compute the power provided or absorbed by the voltage and current sources of Figure 10.7 without making the assumption that $R_1 = I_L = 0$.

Exercise 10.4 Much useful information can be gleaned from device datasheets. This exercise considers just three examples for the TI LMR62014 discussed in Example 10.20:

• By the figure on page 2 of this datasheet, what values of R_1 and R_2 are recommended for the voltage divider to implement feedback (into the device FB pin) that boosts the output to $V_{\text{out}}^{\text{mean}} \approx 12\,\text{V}$?
• By the figure on page 1 of the datasheet, what power efficiency is anticipated for $V_{\text{in}} = 5\,\text{V}$, $V_{\text{out}}^{\text{mean}} = 12\,\text{V}$, and a load of $R = 250$ ohms?
• By page 9 of the datasheet: what is the purpose of the input capacitor C1 in the TI LMR62014 circuit?

Exercise 10.5 (a) Compute the transfer function $V_{\text{out}}(s)/V_{\text{in}}(s)$ of the passive circuit shown in Figure 10.37a, making the same two assumptions as in Example 10.2. Assuming $L\,C = 1$ and $R\,C = 0.5$, plot its Bode plot. What is the cutoff frequency and damping of this filter? (b) Compute the transfer function $V_{\text{out}}(s)/V_{\text{in}}(s)$ of the active circuit shown in Figure 10.37b, again making the same two assumptions as in Example 10.2. Assuming $R_1 = 10$ kΩ and that the op amp is ideal with amplification $A \to \infty$, what values of $\{R_2, C_1, C_2\}$ result in the same frequency response as the passive filter considered in part (a)? Assuming all of the components are readily available (they are!), what advantages does a circuit of the type considered in part (b) have over the circuit considered in part (a)?

(c) Note that a fourth-order low-pass filter may be constructed simply by cascading together two second-order active low-pass filters of the type considered in part (b). Following the development in §9.4.2.1, design an active fourth-order low-pass Butterworth filter and an active fourth-order low-pass Bessel filter, both with $\omega_c = 100$ Hz. Specify the resistor and capacitor values used in each design.

(d) In the active circuit considered in part (b), replace the resistors with capacitors and the capacitors with resistors. Compute the corresponding transfer function and discuss.

Exercise 10.6 Example 10.26 developed a flexible general-purpose *inverting* first-order filter. Sketch the Bode plots of the nine filters that the circuit in Example 10.26 reduces to in the nine special cases enumerated. Then, develop a similarly flexible *noninverting* first-order filter, which is a bit more involved. Start by performing a careful analysis of the circuit in Figure 10.37c, and describe which of the nine cases itemized in the inverting case (Example 10.26) are realizable with this noninverting circuit. Identify precisely what limitations (if any) are present in each case. Reviewing the three special cases considered in Example 10.24, describe precisely how the limitations of this circuit may be circumvented by reconnecting it appropriately.

Exercise 10.7 The circuit in Figure 10.37d (cf. Figure 10.27a) has a transfer function of

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = -K\frac{(s/z_1+1)(s/z_2+1)}{s}\cdot\frac{1}{(s/p_1+1)(s/p_2+1)},$$

and thus may be interpreted as an inverting PID filter combined with two first-order low-pass filters. Determine how each of the variables $\{K, z_1, z_2, p_1, p_2\}$ depend on $\{R_1, R_2, R_3, C_1, C_2, C_3\}$ (show your work, or provide the symbolic code you write to solve the problem for you). Then, solve for $\{R_1, R_2, C_1, C_2, C_3\}$ in terms of $\{K, z_1, z_2, p_1, p_2, R_3\}$.

Exercise 10.8 Replace $\{C_1, C_2, L_3\}$ with $\{L_1, L_2, C_3\}$, respectively, in Example **??** (that is, replace the capacitors with inductors, and replace the inductor with a capacitor, thereby forming a **Hartley oscillator**), and repeat the example in its entirety, following closely the same analysis.

References

Carter, B, & Mancini, R (2009) *Op Amps For Everyone*. Texas Instruments.

Jakas, M, & Llopis, F (2007) LC Sine-Wave Oscillators Using General-Purpose Voltage Operational-Amplifiers, The International Journal of Electrical Engineering & Education **44** (3), 244-248.